Chapter Low power and low area multiplier and accumulator block for efficient implementation ...

Low power and low area multiplier and accumulator block for efficient implementation of FIR filter

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Abstract

In communication system applications, the need for efficient design and implementation of the Finite Impulse Response (FIR) filter is essential. Realization of such a filter with high bit width is a challenging task. The multiplier and accumulator blocks of FIR filter take more delay, power, and area. In this article, design of the FIR Filter using the efficient multiplier and accumulator blocks is presented. We propose to use the operations such as right shift, left shift, and carry save adder to develop FIR filter. The multiplication and division are performed using the right shift and left shift operation. The FIR filter using the Modified Constant Shift Method (MCSM) multiplier block instead of a conventional multiplier is proposed. The modified multiplication in decreases the quantity of hardware, power consumption, and surge the performance of the filter architecture. The FIR architecture is implemented using Xilinx Vivado. The parameter such as the look up table (LUT) count, slices, flip flops, power, and speed are analyzed with respect to existing filter architectures. Thus the proposed novel filter architecture is implemented with high speed, less area, and less power.

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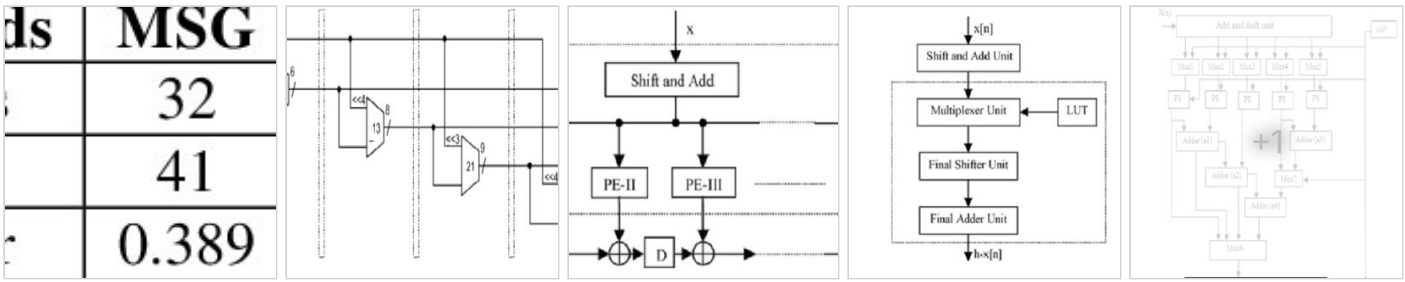

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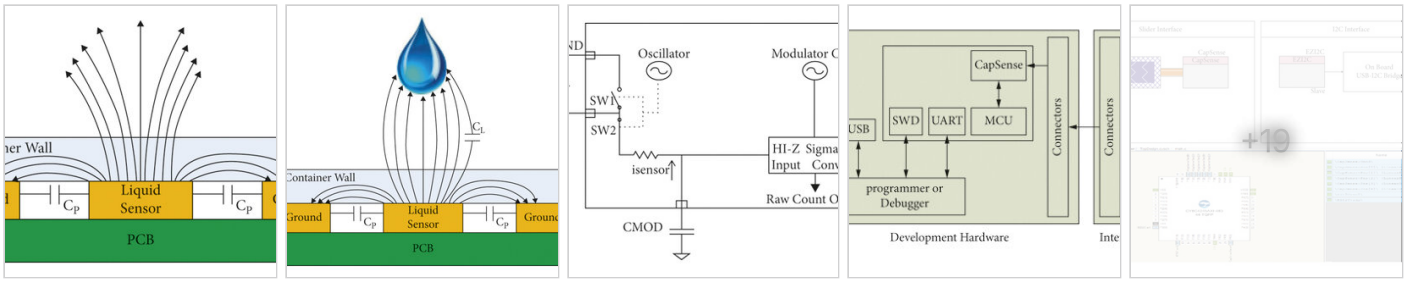

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