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# Passive Island Detection Method Based on Sequence Impedance Component and Load-Shedding Implementation

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**Abstract:** Active islanding detection techniques majorly affect power quality due to injected harmonic signals, whereas passive methods have a large non-detection zone (NDZ). This article presents a new method based on the resultant sequential impedance component (RSIC) as a new approach to island detection with zero NDZs. The abrupt variable in the conventional impedance approach was replaced by the RSIC of the inverter in this method. When the measured value exceeds the threshold range, islanding is detected by monitoring the variations in the RSIC at the point of common coupling (PCC). For proper power utilization in the identified islands, a priority-based load-shedding strategy is also recommended and implemented in this article. Its efficacy was verified in a wide range of real-world settings. It offers superior stability in various non-islanding (NIS) scenarios to prevent accidental tripping. The proposed method advantages include a cheap cost, the simplicity of implementation, independence from the number and type of distributed generation (DG) units connected, and no power quality effects. Compared to other methods reported in the literature, the obtained detection times illustrate that the proposed method is superior.

**Keywords:** islanding detection; distributed generation; non detection zone; load shedding



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## 1. Introduction

As a potential remedy to environmental issues, DG from alternative energy is of great interest to power industry professionals. Integrating DG networks presents several security and protection challenges [1]. DG continues to operate without power grid access, leading to the islanding problem. If the DG cannot maintain voltage and frequency on its own, the system could experience a reduction in stability and power quality [2] due to the negative effects of extensive islanding resulting from DG penetration. An island is created when a DG is disconnected from the grid but its charges remain plugged into the local area. This occurs because this portion of the grid becomes disconnected from the remainder of the system. This phenomenon poses a significant hazard to the safety of users, the grid, and the islanded inverters [3]. For the protection of consumers and infrastructure, the early detection of an islanding situation is crucial [4]. There are three primary categories of islanding detection techniques [5]: communication-based, passive, and active methods. Power line connection, supervisory control, and data collection are remote techniques that rely on bidirectional communication between utilities and DGs [6], which require a reliable communication link. This method has an advantage because, it has less NDZ, but implementing it is expensive [7]. Variable load situations, switching events, and fault events are some of the reasons for islanding detection method failure [8]. Active and passive approaches can be applied to local techniques [9]. The backbone of passive methodologies is the local measurement and comparison of DG properties to reference values. Popular passive approaches include over/under frequency/voltage protection, phase jump detection, and voltage harmonics monitoring [10]. The NDZ for these techniques is quite large. Active approaches with a low NDZ are acquiring popularity these days. When the grid becomes unstable due to the injection of disturbances into the system inverter control, islanding is recognized in these techniques. Active approaches gain irreversible advantages, such as a reduced NDZ and a quicker time taken to detect. Voltage shift, negative sequence current injection [11], slip-mode frequency shift [12], and Sandia frequency [13] are examples of active methods [14]. Although the NDZ for active approaches is minimal, there is a significant risk of false detection when multiple DGs are present because the injection parameter will overlap with non-islanding events [15].

Compared to passive methods, the NDZ is typically smaller in active islanding detection methods, which are based on the deliberate injection of perturbations that cause the voltage magnitude or frequency to stay outside of the established thresholds [16]. The combination of active and passive approaches has facilitated the evolution of hybrid detection methods. The original characteristics of the combined techniques determine the efficacy of hybrid methods. The islanding detection approaches that have been developed up until now have several drawbacks, which the hybrid methods intend to compensate for [17]. As a direct result of this, hybrid techniques are gradually being updated, and it is possible to evaluate them as a tradeoff between the benefits of the original methods and the increasing complexity of their implementation. Some of these approaches include the improved active frequency drift anti-islanding detection method [18] and reactive power injection and ROCOF [19]. The recent passive method for detecting islanding in less than 300 ms [20] utilizes the ripple spectrum content of the voltage at the PCC. Unlike passive and active systems, it is highly dependable, can detect islanding even when there is no variation in power, and is easy to install. Because the ripple content is highly dependent on the inverter's operating frequency, adding a high-powered inverter to the grid could increase the disturbance in the instantaneous output voltage measured by the PCC, resulting in delayed detections. In several patents and published methodologies, techniques for measuring impedance have been used to identify islanding. Examples of these techniques include "signal injection" and "variations in voltage and frequency" [21–23].

In [24], it was determined that injecting a single non-harmonic frequency into a circuit was a reliable method for determining its impedance. The non-harmonic frequency injection method has proven to be effective; however, it has a number of drawbacks, including complex integration, high injection power requirements, disruptive injections, and a costly interface with the power network. This research also employs an approach based on impedance measurements; however, rather than testing at other frequencies, we test at the fundamental frequency by exploiting unbalanced conditions already present in the power network or by injecting small unbalanced signals. Prior to this, both islanding detection and impedance measurement employed similar strategies founded on utilizing unstable situations. Karimi [25] described injecting and measuring a negative-sequence current for simulated islanding detection using a controlled voltage source inverter. By injecting a negative-sequence current of 2% to 3%, islanding detection in less than 60 ms (3.5 cycles) was made practicable. Monitoring the integrity of an onboard impedance network using an unbalanced source is also possible [26,27]. In conclusion, various passive islanding detection techniques are unsuitable for situations where the power output from DG and power input from loads are identical. Non-islanding scenarios such as switching loads or short circuit faults can also fail the majority of algorithms. There have been passive and active approaches to resolving this issue; however, the active approaches risk degrading the system's power quality by introducing noise that is not required. Hybrid systems provide a more dependable and effective performance than active and passive methods, but at the expense of a prolonged detection time and a greater computational burden. The accuracy can be enhanced by combining signal processing (SP) and artificial intelligence (AI)-based methods with passive-based methods. Nevertheless, retraining AI-based approaches is a significant drawback of these systems, and SP-based techniques may be incapable of reducing the NDZ.

This article proposes a new method for detecting islanding using the variations in the sequence impedance components. The symmetric component method requires monitoring voltage and current fluctuations at the PCC to segment the three-phase current and voltage into sequence components. The islanding can be determined by comparing the nominal impedance sequence components before and after the islanding manifestation. During a perturbation, the impedance sequence component is the ratio of the voltage sequence component to the current sequence component. Unlike other methods, this method does not introduce harmonics that degrade power quality or disrupt the interaction between inverters. The technique can detect isolated islands only two cycles after their formation and has a higher overall detection efficiency. The voltage and current will fluctuate until the remote island state runs steadily, at which point they will be decomposed using the symmetric component approach, as the PCC voltage and current cannot change once an isolated island is formed.

The major contributions of the proposed method include the following:

- This article proposes a new islanding detection method based on a resultant sequential impedance component.
- Even with perfectly matched demand and generation, the proposed criterion can quickly distinguish between an isolated situation and grid-connected mode. In contrast to passive detection approaches, the proposed method does not include an NDZ.
- Without the use of a classifier, the method can detect islanding under dynamic loading situations and consistently discriminate between different scenarios.
- The method has a quicker detection of islanding than in the vast majority of previous studies.
- The availability of renewable energy sources, such as solar and wind, connected via converters additionally validates this islanding detection approach.
- A unique novel load-shedding approach is presented for the proper utilization of energy produced from the renewables after the formation of islanding.

The remaining article is structured as follows. Section 2 covers the IEEE 13- bus test system and the proposed algorithm for the suggested technique. Section 3 presents the results and discussion of the proposed islanding detection technique with load shedding. Finally, Section 4 provides the conclusion and future scope.

## 2. Materials and Methods

### *2.1. Architecture and Control Scheme*

The IEEE power engineering society developed the 13-node distribution test feeder to standardize the testing of distribution networks. The distribution feeder runs at a frequency of 60 hertz and a voltage of 4.16 kV. The test feeder in a distribution system simulates elements, including transmission lines, underground cables, spot loads, distributed loads, capacitors, transformers, and regulators. The modified IEEE 13-node distribution test feeder is illustrated in Figure 1 and explained in more detail in the publication above [28]. In the upgraded test system, DGs like wind and solar PV power plants are connected to the grid via nodes 646, 611, and B675.

### *2.2. Proposed Islanding Detection Methodology*

Symmetrical components in time domain: The concept of symmetric components was first introduced in [29] to study unbalanced ploy-phase networks. An unbalanced three-phase system's steady-state phases ($V_{abc}$) are broken down into a positive $\left(V_{abc}^{1}\right)$, negative $\left(V_{abc}^{2}\right)$, and zero-sequence $\left(V_{abc}^{0}\right)$ collection using this method, as shown in Equation (1):

$$V_{abc}= V_{abc}^{1}+V_{abc}^{2}+V_{abc}^{0} \tag{1}$$

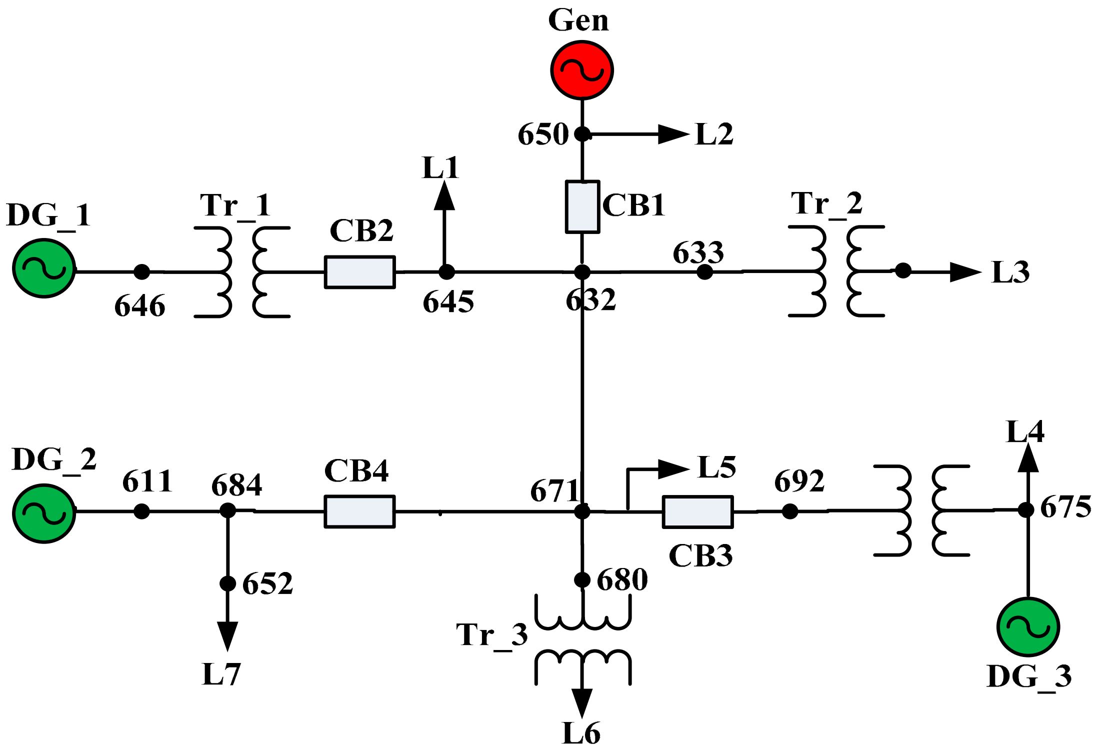


**Figure 1.** System under consideration for proposed islanding detection technique.

As a result, given a standard three-phase voltage matrix, $V_{abc}$, as shown in Equation (2), we can derive the phase "*a*" symmetric components via the equation $Vs = TV_{abc}$, where $Vs = \left[V_a^1, V_a^2, V_a^0\right]^T$ and $T$ is the transformation matrix.

$$\begin{bmatrix} V_a^1\angle\theta_a^1 \\ V_a^2\angle\theta_a^2 \\ V_a^0\angle\theta_a^0 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} V_a\angle\theta_a \\ V_b\angle\theta_b \\ V_c\angle\theta_c \end{bmatrix} \quad (2)$$

where $a = e^{j120^o}$.

Phase *b* and *c* have the following sequence components shown in Equations (3)–(5):

$$V_b^1 = a^2 V_a^1 : \; V_c^1 = aV_a^1 \quad (3)$$

$$V_b^2 = aV_a^2 ; V_c^2 = a^2 V_a^2 \quad (4)$$

$$V_a^0 = V_b^0 = V_c^0 \quad (5)$$

Resultant sequence impedance component (RSIC): One difficulty with impedance-based islanding detection is determining the equivalent impedance at the common point. The inverter causes a change in the system's characteristic current, and the non-characteristic harmonic voltage is then measured to establish the system's impedance to these harmonics. The conventional approach has two significant flaws: (1) it compromises power quality under normal conditions of use by injecting harmonic current into the system; (2) the parallel operation of the multi-inverter results in mutual influence from the harmonics injected by each inverter. These could lead to more mistakes or blind spots. Conventional impedance islanding detection relies on a sudden amplitude transition. This strategy fails if the power supplied by the microgrid system and the power needed by the load are not adequately matched. Microgrids are subsystems of distribution networks and are inherently unstable. Disconnecting a microgrid from the main grid while using inverters and rotation-based DGs causes voltage, current, and impedance sequence components to change from standard values. From Equation (2), the voltage and current for a positive, negative, and sequence impedance can be expressed as in Equations (6)–(9).

$$V_a^2 = \frac{1}{3}\left(V_a + a^2 V_b + aV_c\right) \tag{6}$$

$$I_a^2 = \frac{1}{3}\left(I_a + a^2 I_b + aI_c\right) \tag{7}$$

Negative sequence impedance can be written as (8):

$$Z_2 = \frac{V_a^2}{I_a^2} \tag{8}$$

Similarly, positive sequence impedance is shown below (9):

$$Z_1 = \frac{V_a^1}{I_a^1} \tag{9}$$

The sum of positive and negative sequence impedance as $Z_{norm}$ is shown in Equation (10):

$$Z_{norm} = Z_1 + Z_2 \tag{10}$$

The resultant impedance sequence component is calculated from the absolute output of the difference measured ($Z_{inst}$) and normal impedances ($Z_{norm}$) at the PCC in Equation (11):

$$\text{RSIC} = |\ (Z_{norm}) - (Z_{\ inst})| \tag{11}$$

where $Z_{inst}$ is the sum of instantaneous impedances of positive and negative sequence components. The identification of islanding is assumed to be faster and more accurate using a system that can differentiate between islanding and non-islanding scenarios. For this reason, the suggested detection method uses both positive and negative sequence impedance components. The three-phase voltages and currents at the PCC (node 650) are analyzed to determine their values.

To acquire the output, we fed the collected signals into a sequence analyzer and used Equation (11) to calculate the absolute difference in impedance sequence component between the measured output and grid-connected instances as the RSIC. A constant value can be obtained by calculating the mean and then comparing it to the threshold. The islanding detection waveform (IDW) is set to logical 1 by the timer if the mean of the RISC takes longer than the threshold. Whenever the non-islanding measured RISC mean falls below the threshold, the IDW remains in the logical '0' state. The proposed algorithm is depicted in block diagram form in Figure 2.

### *2.3. Load Shedding (LS)*

Because of the power disparity on the island, load management is challenging. Most current control schemes use load shedding (*LS*) as a corrective mechanism to keep the island operating smoothly. A load-shedding strategy based on priority is developed to maintain the power balance on the discovered island. The proposed load-shedding procedure is initiated when the island's power demand exceeds the supply from its DG sources. Frequency and voltage variations over time are used to rank the burdens. The bus with the greatest fluctuations in voltage and frequency is the best candidate for load shedding. Because the frequency and voltage fluctuations at the DG bus are less severe than they would be without DG, the DG bus is exempt from load curtailment. All remaining buses are rated and their burdens are reduced until the system frequency and voltage of the buses return to acceptable levels. Based on the rank and loading of the individual buses, Equation (12) expresses the total quantity of burden discharged in the system:

$$LS = PC_k\ * P_{load,k} \tag{12}$$

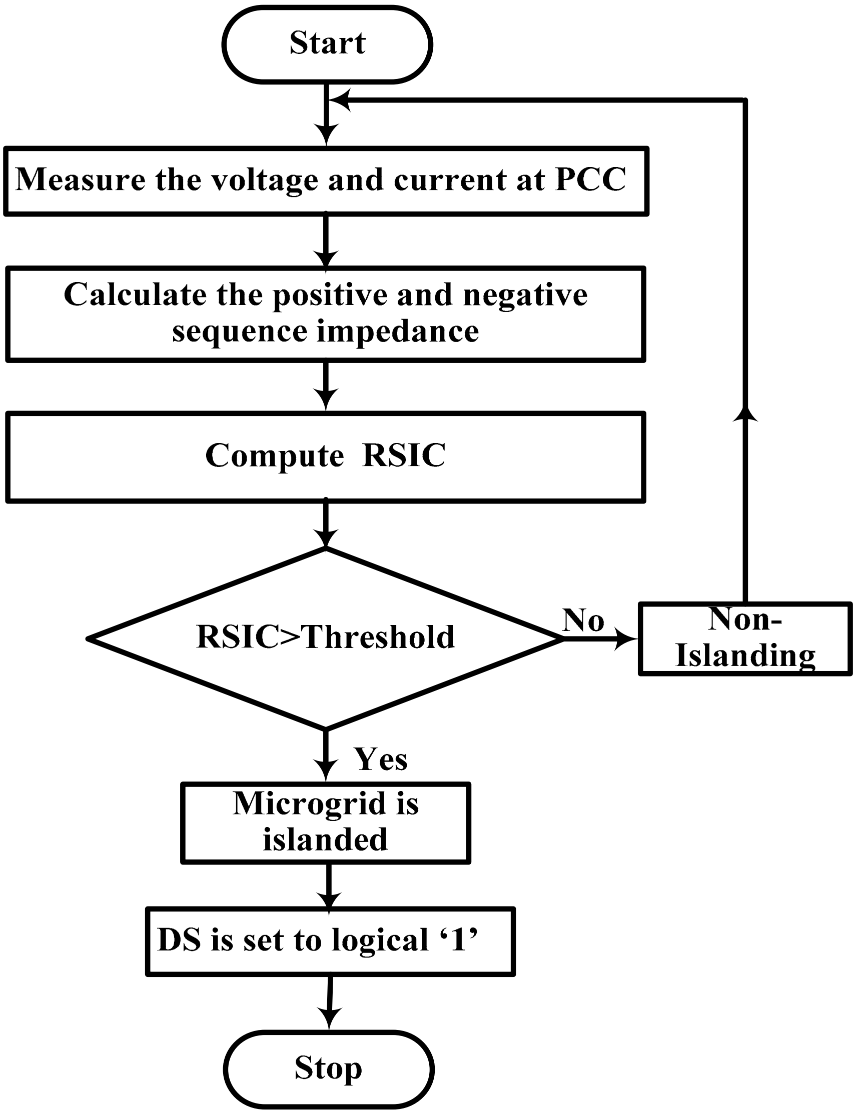


**Figure 2.** Flow chart of the proposed detection technique.

$PC_k$ is the parity coefficient for a given bus, and it is found using Equation (13), when $P_{load,k}$ is the load on bus '*k*':

$$PC = D_k * \beta_f * \beta_v \tag{13}$$

where $\beta_f$ and $\beta_v$ are the frequency and voltage aspects of the buses, computed using Equations (14) and (15):

$$\beta_f = \frac{f_{k,t}}{f_{int,0}} \tag{14}$$

$$\beta_v = \frac{v_{k,t}}{v_{int,0}} \tag{15}$$

When load shedding is commenced, the frequency at bus '*k*' is $f_{k,t}$, and when islanding is identified, the initial frequency at bus is $f_{int,0}$. Bus '*k*' voltage $v_{k,t}$ is measured at the time load shedding begins; bus 'initial' voltage $v_{int,0}$ is measured at the time islanding is identified. Each bus's load shedding in a distribution system is on or off; hence, $D_k$ is always either 0 or 1 as presented in Equation (16):

$$D_k = \begin{cases} 0, \ if\ DG\ is\ present \\ 1, \ DG\ is\ absent \end{cases} \tag{16}$$

Before and after load shedding, the isolated system's dependability is measured to determine the efficacy of the proposed priority-based load-shedding technique. The reliability analysis is conducted using conventional reliability indices, line failure rates, and repair schedules. SAIDI, SAIFI, CAIDI, ENS, and AENS are well-known examples of reliability indices. Notifications of client failures are a common source for these metrics [20]. The quantitative reliability analysis of the system measures the impact of the proposed load-shedding scheme. Before and after the load-shedding process, standard reliability indices such as SAIDI, SAIFI, CAIDI, ENS, and AENS are used to evaluate the performance of the proposed load-shedding scheme. Because this research depends on the number of afflicted consumers, the effect of emergency load-shedding systems can be measured using conventional reliability indices. Indicators of power outage reliability include a list of affected customers. Figure 3 visually represents the priority-based load-shedding technique described in [30].

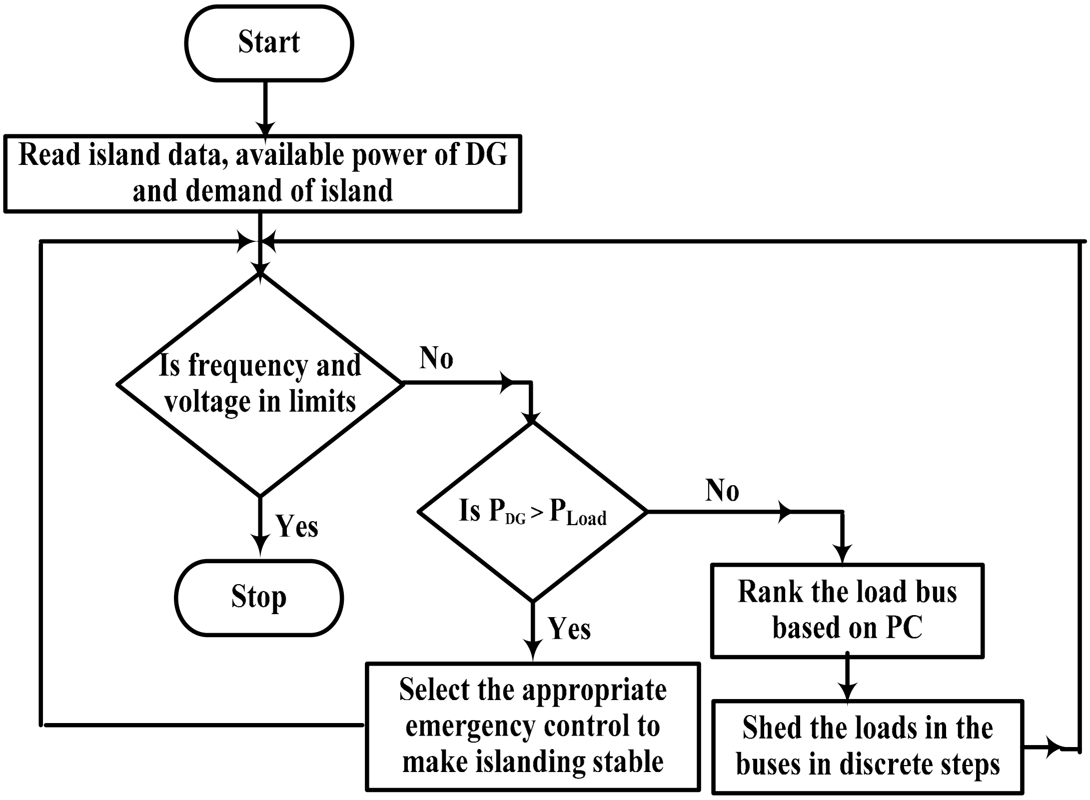


**Figure 3.** Flowchart of proposed priority-based load-shedding method.

## 3. Results and Discussion

### *3.1. Islanding (IS) Cases*

#### 3.1.1. Variation in Load Quality Factor

Load quality (Q.F) factors between 1 and 2.5 are evaluated for islanding detection in accordance with IEEE standards. The results of the RSIC with a varying load quality factor and no power mismatch are displayed in Figure 4a. The magnitude difference between the grid-connected and islanding RSIC can be reduced by raising the load quality factor. A higher Q.F indicates a higher load of reactance, which reduces the frequency of oscillations in the voltage and current waveforms following islanding. The ISDW reveals a phenomenon analogous to island life in all its forms. In this work, the load quality factor for islanding scenarios is set at 2.5 and, for non-islanding scenarios, it is set at 1.0. The trigger signal is depicted in Figure 4b. The suggested approach guarantees reliable islanding detection even at the extremes of the typical load quality factor.

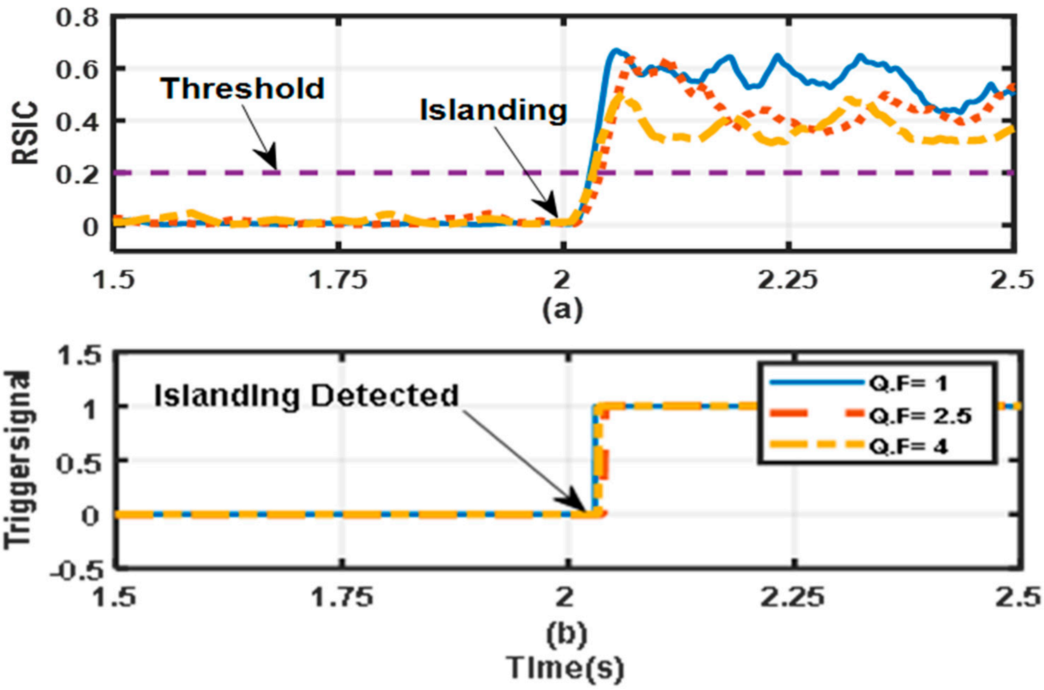


**Figure 4.** (**a**) RSIC for the impact of varying quality factor. (**b**) Trigger signal.

3.1.2. Imbalance in Real Power

Real power imbalances between the DG power and the load power are shown by the RSIC variations in Figure 5a. When the breaker opens at 2 s, the RSIE amplitude is larger than the initial value. If the real power discrepancy is positive, the DG power will be higher than the load power, and vice versa if the mismatch is negative. Cases where real power is increased or decreased by 2% to 20% are explored. If there is more than a 20% difference in power use, the voltage levels are outside the NDZ. That is why we settled on a value of 20% for the most significant possible power disparity. The trigger signal is depicted in Figure 5b.

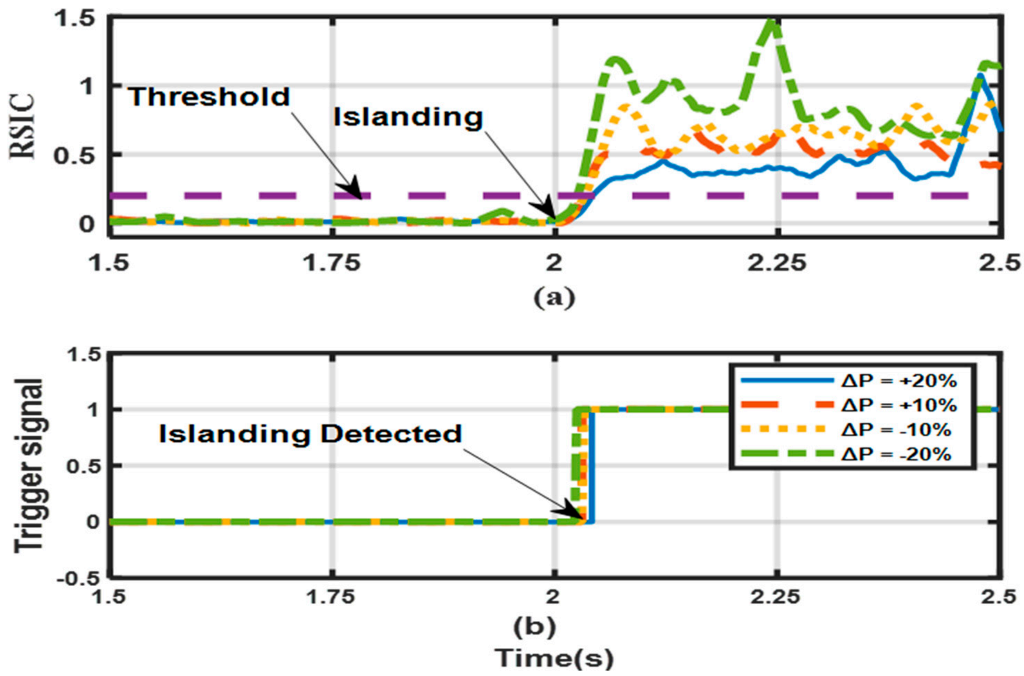


**Figure 5.** (**a**) RSIC for the impact of varying real power, (**b**) Trigger signal.

Imbalance in reactive power: the RSIC signal for reactive power imbalance for the inductive and capacitive load is shown in Figure 6a, respectively. When the breaker opens at 2.0 s, the detecting signal (RSIC) amplitude is larger than the threshold level. In this way, the islanding condition is recognized by the algorithm. Consider the case of a positive reactive power mismatch in which the capacitive demand is lower than the inductive demand. The range of reactive power variances from 0.2% to 2% is considered to analyze both the increase and decrease in reactive power. When the reactive power imbalance is greater than the +2% and −2% thresholds, islanding is identified and the frequency deviates from the NDZ. The trigger signal is depicted in Figure 6b.

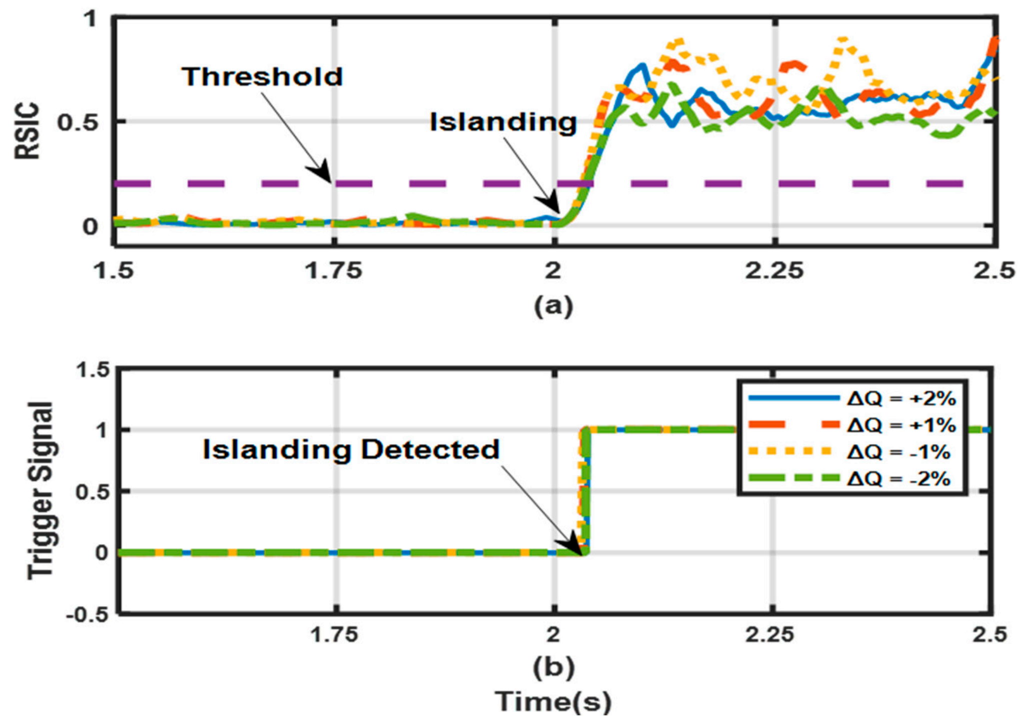


**Figure 6.** (**a**) RSIC for the impact of varying reactive power. (**b**) Trigger signal.

### *3.2. Non-Islanding Cases*

#### 3.2.1. Short Circuit Faults

Simulations of three-phase faults (LLLs), two-phase faults (L.L.s), and phase–ground faults (L.G.) are all possible. When the circuit breaker in the parallel feeder trips, the fault gets fixed in less than two seconds. The fault resistance is adjusted between 1 and 75 ohms in each scenario. Figure 7a depicts the RSIC fault-detection signal for LLL, L.L., and L.G. faults. Figure 7b shows that the detection signal magnitude was below the threshold for all fault categories, indicating that no false detections occurred.

#### 3.2.2. Capacitor Switching

At 2.0 s, the capacitor bank turns on and goes from 10% to 100% in steps that last 0.02 s each. With the same 0.02 s interval between each step, the capacitor banks are discharged from 100% to 10% after 2.5 s. Figure 8a depicts the islanding detection signal for 100% capacitor bank switching. As demonstrated in Figure 8b, a false trip can be avoided by using a suitable threshold, as the peak in these switching circumstances quickly saturates and has a value below the threshold.

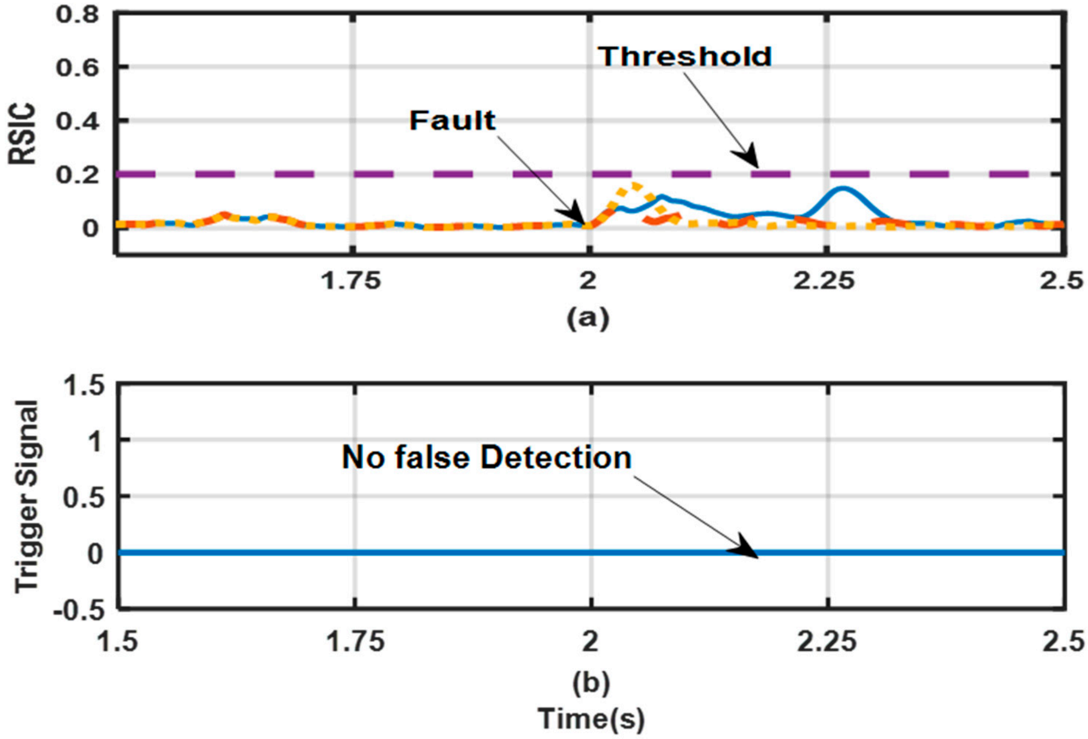


**Figure 7.** (**a**) RSIC for the short circuit faults. (**b**) Trigger signal.

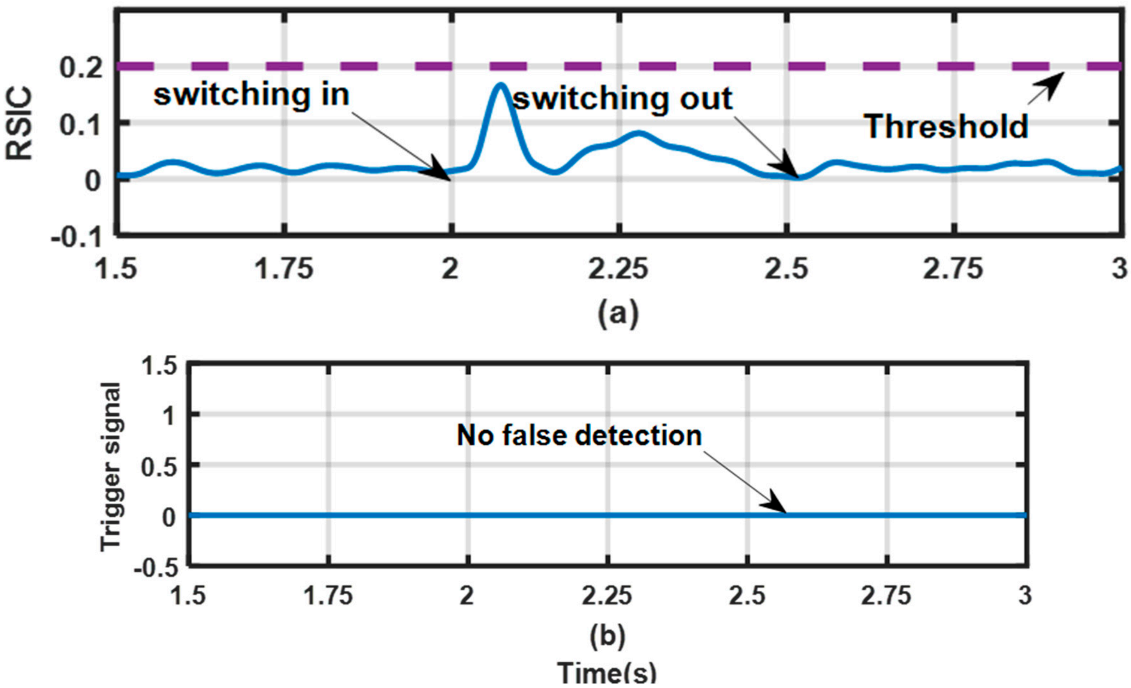


**Figure 8.** (**a**) RSIC for the 100% capacitor bank switching. (**b**) Trigger signal.

3.2.3. Load Switching

In this scenario, we think about turning loads on and off. At 2.0 s, the load is activated, and from there it is gradually increased in 10% increments up to 100%, with each increment lasting 0.02 s; starting at 2.5 s, the load is gradually decreased from 100% down to 10%, also in 10% increments. For full load switching, the islanding detection signal (RSIC) is displayed in Figure 9a. Since the RSIC signal is flat throughout load switching, the detection signal returns to normal values lower than the threshold, preventing an incorrect islanding detection (Figure 9b).

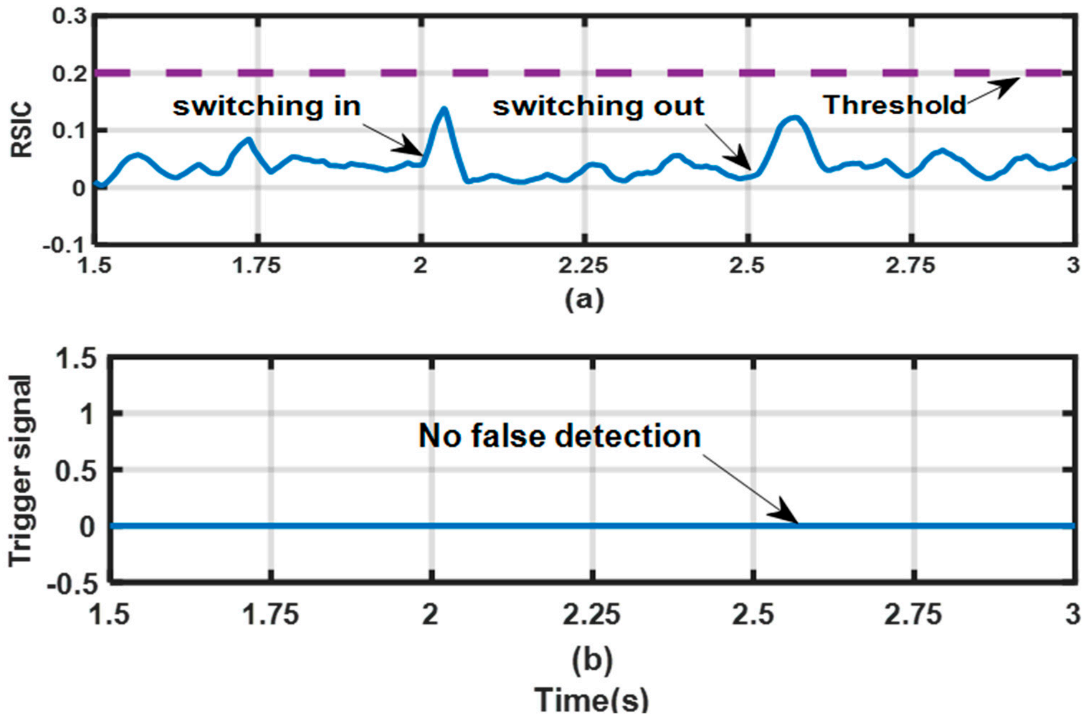


**Figure 9.** (**a**) RSIC for the 100% load switching. (**b**) Trigger signal.

### 3.2.4. Load Shedding

Before as well as following load shedding using the suggested priority-based strategy for the 13 bus system, the voltage and frequency parameters of the islanded bus are depicted in Figure 10a,b, accordingly. Islanding occurs at 0.3 s and the load-shedding algorithm starts at 0.5 s, making the system's voltage and frequency stable at 0.8 s. In Table 1, the load-shedding order for the priority-based load shedding is shown. Table 2 presents the comparative assessment of various techniques used in literature with the proposed method in terms of NDZ, quality factor, need for delay and load shedding implementation.

**Table 1.** PC-based demonstration of load ranking.

| Load Ranking Based on PC | Load Number | Load Demand (kVA) | Type of Load |
|---|---|---|---|
| 1 | 5 | 420 + j200 | Heavy load |
| 2 | 8 | 400 + j200 | Heavy load |
| 3 | 7 | 310 + j1600 | Heavy load |
| 4 | 4 | 300 + j160 | Heavy load |
| 5 | 9 | 130 + j90 | Heavy load |
| 6 | 1 | 75 + j40 | Light load |
| 7 | 11 | 75 + j35 | Light load |
| 8 | 10 | 75 + j30 | Light load |
| 9 | 6 | 60 + j35 | Light load |
| 10 | 2 | 60 + j30 | Light load |
| 11 | 12 | 60 + j25 | Light load |
| 12 | 3 | 40 + j25 | Light load |

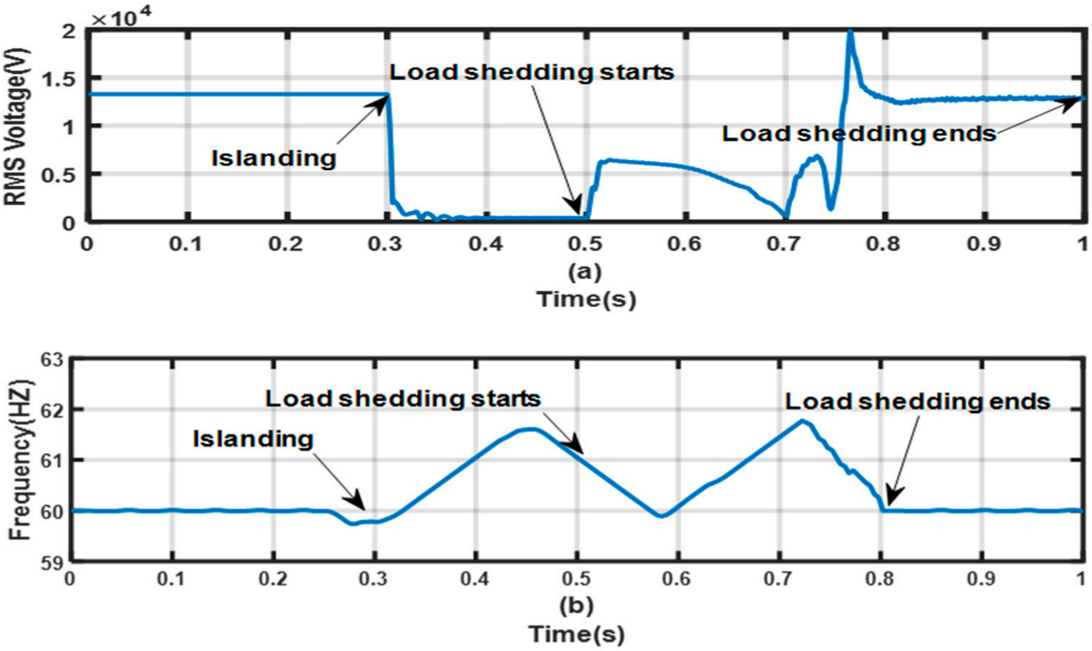


**Figure 10.** (**a**) RMS voltage. (**b**) Frequency for load shedding.

**Table 2.** Comparison to the literature.

| Reference | Q.F | Detection Time (ms) | NDZ | Need of Time Delay | Load Shedding |
|---|---|---|---|---|---|
| [1] | 1 | >340 | Small | 50 ms | No |
| [20] | 1 | >300 | Small | 80 ms | No |
| [27] | 2.5 | <350 | Small | 150 ms | No |
| [31] | 0.96 | <454 | Small | No | No |
| [2] | 2.5 | >325 | Small | 100 ms | No |
| [21] | 2.5 | >315 | Small | 100 ms | No |
| [22] | 2.5 | >200 | Medium | No | No |
| [23] | 2.5 | >350 | Small | No | No |
| Proposed | 1 | 31.2 | Zero | No | Yes |
| | 1.5 | 32.6 | | | |
| | 2 | 34.5 | | | |
| | 4 | 32.2 | | | |

## 4. Conclusions

This paper presents a novel passive islanding detection approach based on the measurement of voltage and current at the PCC and using an RSIC for islanding detection. Using the provided technique, islanding could be detected in roughly 30 milliseconds. Several island scenarios were used to verify the effectiveness of the proposed methods. The suggested method successfully distinguishes between islanding and non-islanding scenarios. This method can also determine the most optimal threshold value, even if the RSIC varies for reasons other than islanding.

An adjustable PC parameter is used for the island's proposed priority-based load-shedding system to determine which buses will be affected. The proposed solution requires less load shedding to restore the frequency and voltage stability on the island than the standard load-shedding strategy. Before initiating load shedding, the proposed PC parameter considers the availability of DG units, frequency, and voltage fluctuations on a bus. In future, the work can be extended with real-time simulators and real systems.

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