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Fuzzy Logic Controlled Current-Mode Switch Mode Power Supply with Enhanced Steady State Response

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Abstract: Switched mode power supplies are widely employed nowadays in a variety of sensitive and electronic equipment that needs a more reliable, permanent power source. The modeling and simulation of an Interleaved Flyback Switched Mode Power Supply (IFSMPS) system with Power Factor Correction (PFC) is described. This study suggests using a fuzzy logic controller to interleave fly-back converters to produce the necessary DC voltage. Systems controlled by fuzzy logic and closed-loop fractional order PID (F.O.P.I.D) are simulated, and the results are compared. The results show that the CMC-FLC based system outperformed the CMC-FO.P.I.D controlled IFSMPS system in terms of dynamic response.

Keywords: *Interleaved Flyback Switched Mode Power Supply (IFSMPS), Current Mode Control (CMC), Dynamic performance, F.O.P.I.D Controller, Fuzzy Logic Controller, Machine tool Application.*

1. Introduction

In the Current scenario, Switched Mode Power Supply (SMPS) is designed with enhanced Power Quality (PQ) as a result of harmonic pollution awareness. Currently, Personal Computer (PC) has played a major role in our day-to-day life. Generally the power supply of a Personal Computer needs many numbers of DC to DC converters for more number of regulated and isolated outputs with enhanced Power Quality [1].As a consequence, the cost and complexity of the system becomes very high. Switching converters are more in demand on the market today because of improvements in semiconductor technology. There are more switching devices available, and they can handle more power and switch at faster speeds. More over the design of switching mode power supplies with less weight, small size and a greater efficiency is feasible [2].

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The power semiconductor devices in these switching converters either operate in on or off state. Since both states cause low switching voltage or current, using a switching regulator, the conversion has to be done with greater efficiency [3-4]. The unpredictable charging and discharging of the capacitor causes a high crest factor, highly distorted, and irregularly heavy input current on the single phase-ac side, which ultimately results in an international power quality violation. The current and power harmonics cause the distortions in input source voltage. To rectify the above hitch, an improved power quality IFSMPS with unity PF has been researched [4-7].

In this paper, fly back converter is selected as there are lesser number of magnetic and semiconductor components as compared to other types of SMPS. The several advantages of this converter are good input-output isolation, simple in construction and cost-effective [8-10].

Various methods have been developed to enhance the Power Quality of the Converter. In this paper a T-Filter is introduced at the front side of the converter in order to eliminate the harmonics and enhance the power quality.

This paper also involves the usage of different types of controllers to achieve the regulated output with quicker dynamic response. If there is any sudden change occurs at the input of the open loop circuit, then the output gets disturbed for a longer time. In order to attain the regulated output within a shorter period of time after a disturbance occurs, closed loop control is introduced [11-14]. Fuzzy logic controlled Interleaved Fly back Switched

Mode Power Supply (IFSMPS) and closed-loop Fractional Order Proportional Integral Derivative (FOPID) systems are simulated, and the findings are connected. This work illustrates various controllers to enhance the dynamic performance of the fly back switched-mode power supply and contributes to a better understanding of control strategies owing to input voltage changes[15-16]. Simulation of IFSMPS is done and the results are related with the hardware output.

2. Description Of System

A closed two-loop IFSMPS with P.I. and F.O.P.I.D. controller's diagram is illustrated in Fig.1.

Basic equation of Switched Mode Power Supply is

$$V_0 = (V_1 * Ton)/ T \quad \text{--- (1)}$$

Where,

V_0 = Output-Voltage

V_1 = Input- Voltage

Ton = On Time

T = Total Time

$$Ton = (V_0 * T)/V_1 \quad \text{--- (2)}$$

RMS value of emf induced in the primary and secondary side is

$$Epr = KN1Pf \quad \text{--- (3)}$$

$$Ese = KN2Pf \quad \text{--- (4)}$$

Where,

K=4.44

N1, N2= Number of turns in the primary as well as secondary respectively

f= frequency

P= Maximum flux in the core

In this paper F.O.P.I.D. controller is used which is evolved from fractional differentiation. The block diagram of Interleaved Fly back Switched Mode Power Supply (IFSMPS) is shown in Fig 1 where F.O.P.I.D. and P.I controllers are used in the inner and outer loop respectively.

The transfer-function of an F.O.P.I.D. controller takes the form of

$$C_{F.O.P.I.D.}(s) = K_P + K_I/s^{\alpha} + K_D s^{\beta} \quad \text{--- (5)}$$

Where α,β represents the order of the integral and derivative parts. K_P, K_I and K_D are the constants of the controller as that of a conventional P.I.D-controller.

The comparison of obtained dc-voltage the reference-voltage is made which generates an error-signal. This error-signal thus obtained is given to P.I. which sustains the output-voltage-constant and diminishes the steady-state-error. The set-current is compared with actual current. Zeigler Nichols tuning is used to evaluate the proportional-gain (Kp) and double-integral-times (Tis) of F.O.P.I.D. parameters.

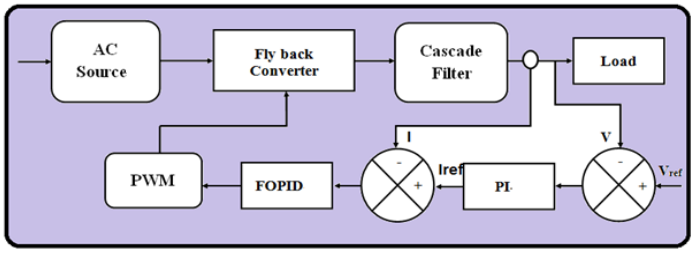

Fig 1. Block Diagram of two loop IFSMPS with P.I. - F.O.P.I.D. controller

Block Diagram of two loop IFSMPS is shown in Fig 2 where FLC controllers are used for both inner and outer loop. The obtained error-signal is coursed by the FLC to sustain the output voltage constant and diminish the steady state error.

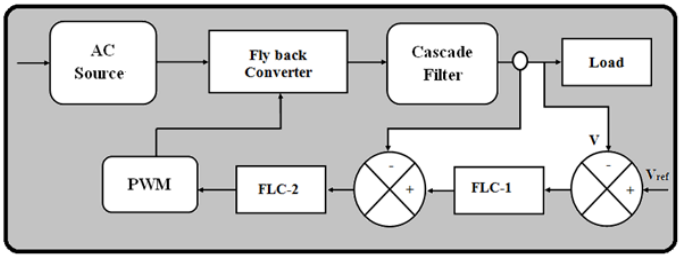

Fig 2. Block Diagram of two -loop IFSMPS with CMC-FLC

3. Results And Discussion

A. IFSMPS system with P.I.-F.O.P.I.D. Controller

Simulation diagram of two-loop IFSMPS s with P.I. - F.O.P.I.D. controller is delineated in Fig 3. Outer-loop of IFSMPS uses P.I.-controller and inner-loop uses F.O.P.I.D. controller. Input voltage of two-loop IFSMPS with P.I. - F.O.P.I.D. controller is given as 400V in Fig 4. Output voltage of Rectifier in IFSMPS is delineated in Fig 5. The value of output voltage of rectifier of IFSMPS is 280V. Output voltage of the IFSMPS with P.I. - F.O.P.I.D. controller is given as 88V in Fig 6. The Output current of the IFSMPS with P.I. - F.O.P.I.D. controller is shown as 1.8A in Fig 7. Output-power of the IFSMPS with P.I. - F.O.P.I.D. controller is given as 180 W in Fig 8. The output current ripple in CMC-IFSMPS is given as 0.002A in Fig 9.

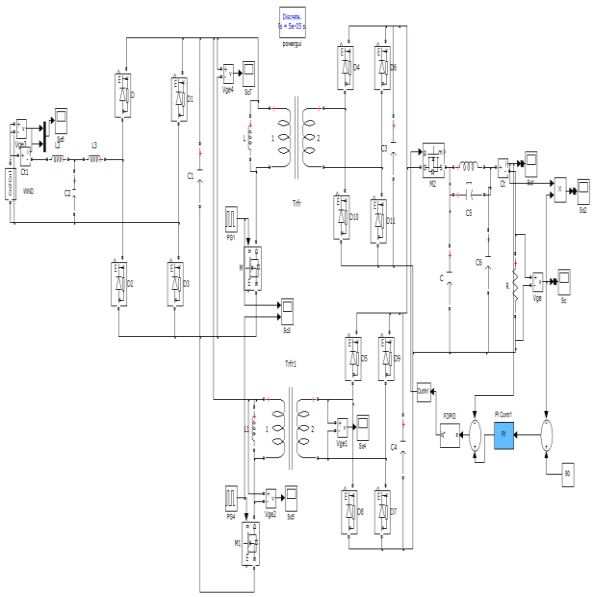

Fig 3. Simulation diagram of the IFSMPS with P.I. - F.O.P.I.D. controller

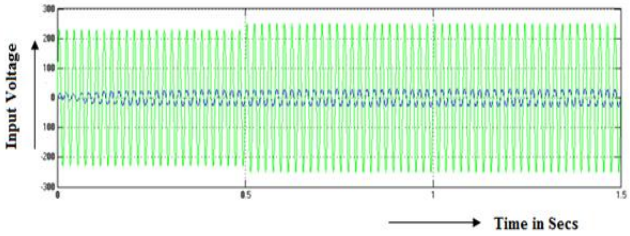

Fig 4.Input voltage

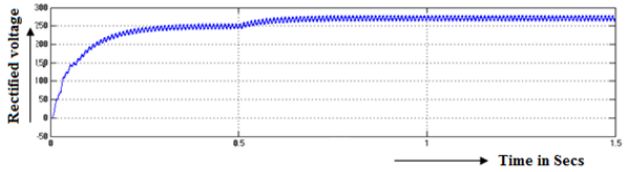

Fig 5. Output voltage of rectifier of the IFSMPS with P.I. - F.O.P.I.D. controller

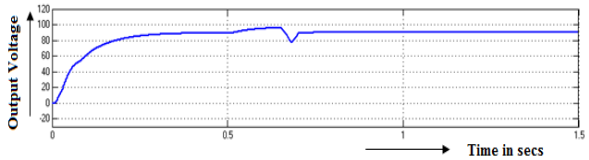

Fig 6. Output voltage of the IFSMPS with P.I. - F.O.P.I.D. controller

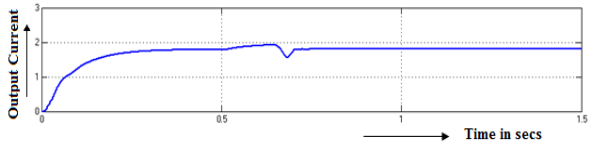

Fig7. Output current of the IFSMPS with P.I. - F.O.P.I.D. controller

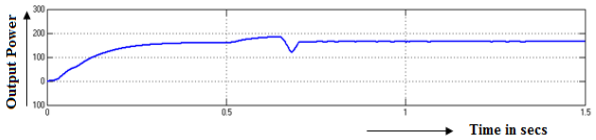

Fig 8. Output power of the IFSMPS with P.I. - F.O.P.I.D. controller

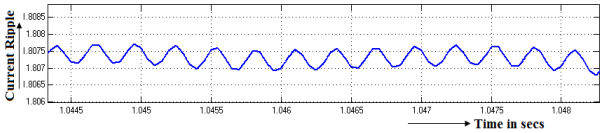

Fig 9. Output Current ripple in the CMC- IFSMPS with P.I. - F.O.P.I.D. controller

B. IFSMPS system with FL Controller

Fig. 10 shows the simulation schematic for a two-loop IFSMPS with a FL controller. Fig. 11 shows the input voltage and current waveforms for the two-loop IFSMPS with FL controller. The source current and voltage can be shown to be in phase. This is a result of T-network being present at the IFSMPS input. 400V is the input voltage value. In Fig. 12, the output voltage of the IFSMPS's rectifier is shown as 280V. The rectifier's output voltage is 280V in value. In Fig. 13, the output voltage of the IFSMPS with the FLC controller is depicted as 90V. In Fig. 14, the output current of the IFSMPS with the FLC controller is depicted as 1.8A.Output-power of CF-SMPS is given as 160W in Fig-15. The output current ripple in CMC-IFSMPS is given as 0.0001A in Fig-16.

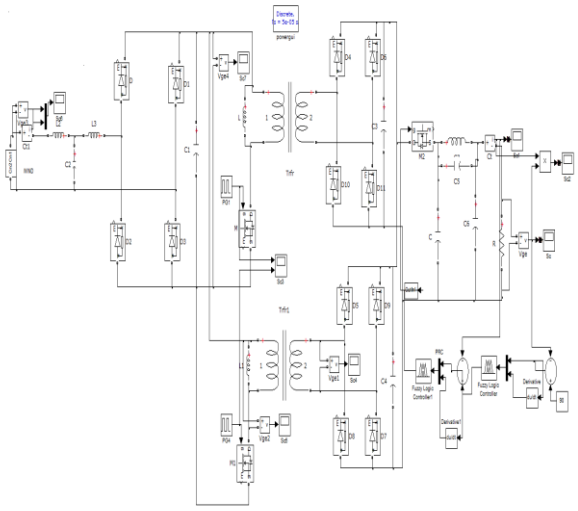

Fig 10. Simulation diagram of the two loop IFSMPS with FL controller

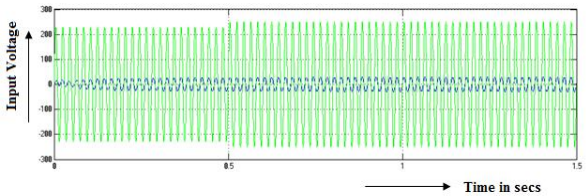

Fig 11. Input voltage

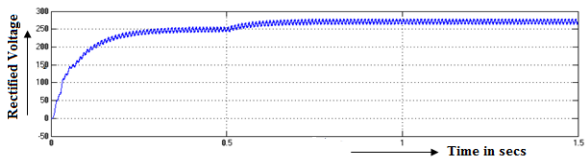

Fig 12. Output voltage of rectifier of IFSMPS with FL controller

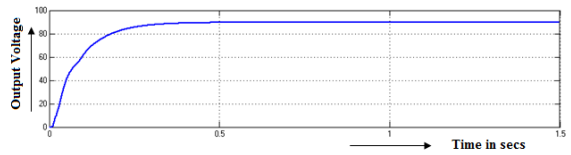

Fig 13. Output voltage of IFSMPS with FL controller

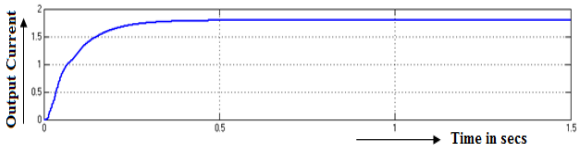

Fig 14. Output current of IFSMPS with FL controller

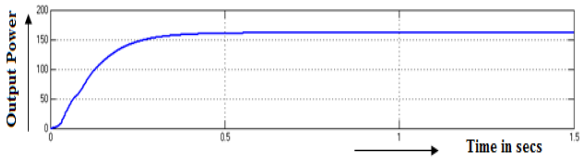

Fig 15. Output power of IFSMPS with FL controller

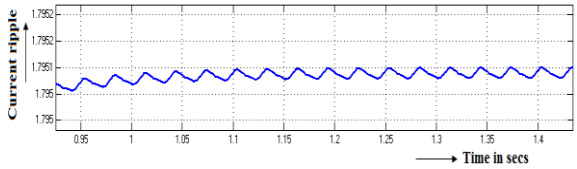

Fig 16. Output Current ripple in the CMC- IFSMPS with FL controller

Comparison of time domain parameters (Voltage) using P.I.-F.O.P.I.D. and FLC-FL controller are given in Table I. It is noted that the FLC-FL reduces the rise time from 0.52 seconds to 0.18 seconds, the peak time from 0.54 seconds to 0.37 seconds, and the settling time from 0.60 seconds to 0.42 seconds.; the-steady-state-error from 1.6V to 0.4V.

Table I
Comparison Of Time- Domain Parameters (Voltage) Of Cf-Smps Using P.I.-F.O.P.I.D And Flc-Fl Controllers

Controller	t_r(sec)	t_p(sec)	t_s(sec)	e_{ss}(V)
P.I. - F.O.P.I.D.	0.52	0.54	0.60	1.6
FLC- FLC	0.18	0.37	0.42	0.4

Comparison of time domain parameters (Current) using P.I.-F.O.P.I.D and FL-FL controllers is given in Table II. It is noted that with FLC-FL rise time reduces from 0.52Sec to 0.19Sec; the peak time from 0.55Sec to 0.35Sec; the settling time from 0.59Sec to 0.40Sec; the-steady-state-error from 1.2A to 0.1A.

Table II
Comparison Of Time- Domain Parameters (Current) Using P.I.-F.O.P.I.D And Fl Controllers

Controller	t_r(sec)	t_p(sec)	t_s(sec)	e_{ss}(V)
P.I.-F.O.P.I.D.	0.52	0.55	0.59	1.2
FLC-FLC	0.19	0.35	0.40	0.1

Comparison of output current ripple using P.I. F.O.P.I.D and FL-FL controllers is specified in Table III. The Output current ripple is reduced from 0.002A to 0.0001A.

Table III
Comparison Of Output Current Ripple Using P.I.-F.O.P.I.D And Cmc-Fl Controllers

Controller	Output current Ripple
PI-FOPID	0.002A
FLC-FLC	0.0001A

4. Experimental Results

The IFSMPS is constructed and put through testing in the lab. Rectifier modules, high frequency inverter, and transformer make up the IFSMPS's hardware. Fig. 15 shows a hardware snapshot. Fig. 16 displays the input voltage's output. Fig. 17 shows the fly-back inverter's switching pulses for M1 and M2. Figures 18 and 19 show, respectively, the primary and secondary voltages of the transformer. Figs. 20 and 21 show output voltage across R-load and output current through R-load. List of hardware components used are furnished in Table IV.

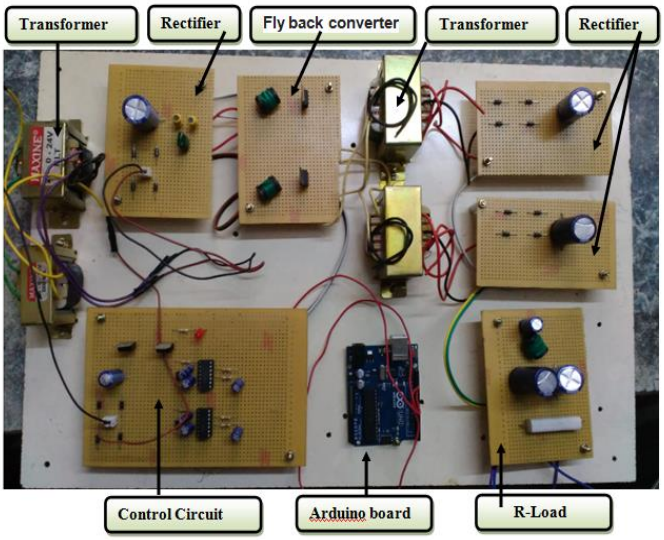

Fig 15 Hardware snap shot of IFSMPS

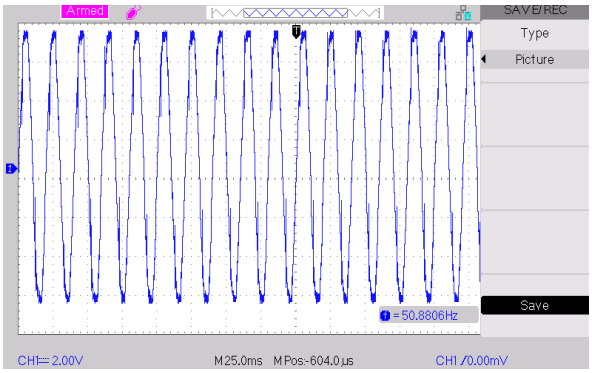

Fig 16 Input voltage

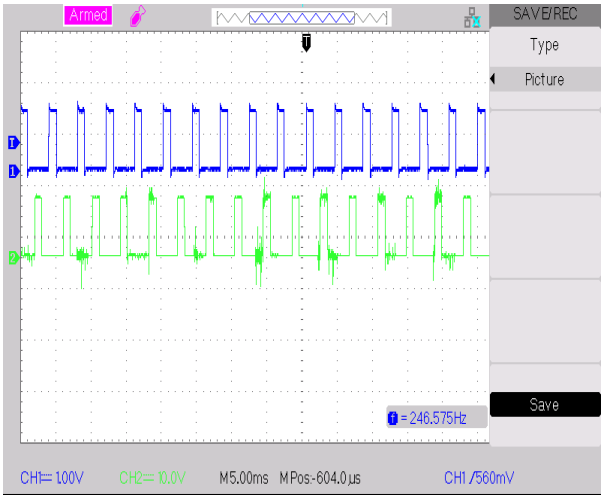

Fig 17 Switching pulses for M1 & M2 of flyback inverter

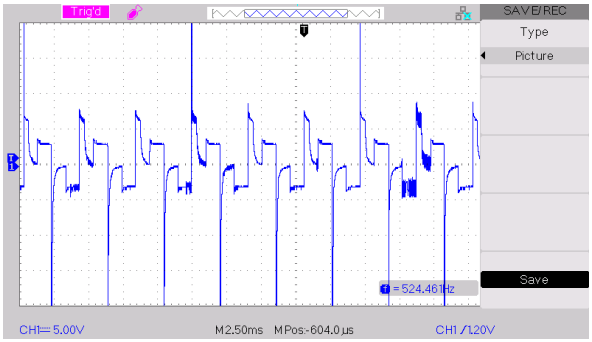

Fig 18 Transformer- primary voltage

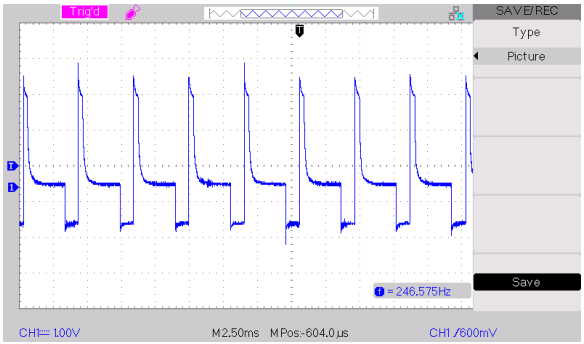

Fig 19 Transformer- secondary voltage

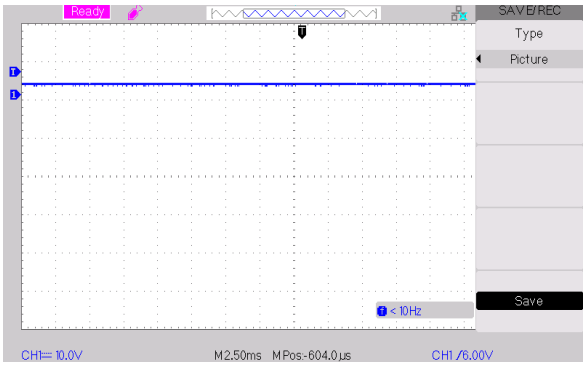

Fig 20 Voltage across R-load

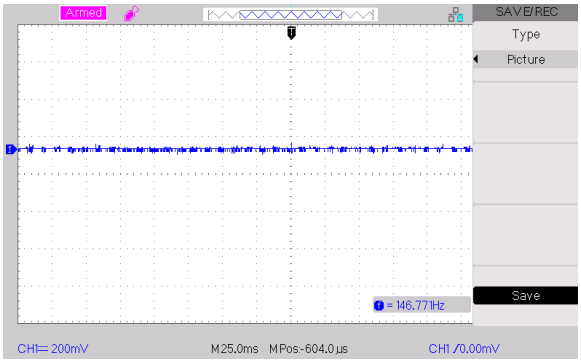

Fig 21 Current through R- load

Table IV

List Of Components Used For Hardware Of Ifsmps

Name	Rating
C	1000E-03, 4.70E-05, 2.20E-03, 3.30E-11
Diode	1000V ,3A
L	10uH
MOSFET (IR840)	600V,8A
R	1k,100K,22K
Regulator	7812, 7805
IC	IR2110
P.I.C controller	P.I.C16F84A

5. Conclusion

The simulation studies of closed-loop IFSMPS with P.I.-F.O.P.I.D and FL-controllers are done using MATLAB Simulink model. The outcomes indicate that the FLC-FL system produced an improved dynamic response in comparison with that the P.I.-F.O.P.I.D controlled IFSMPS system.

The advantages of the suggested IFSMPS system are decreased settling time, low input-current ripple as well as steady state error. By interleaving the fly back converters, the current ripple at the input side can be greatly reduced. Also by using cascade filter at the output side, the output current ripple is reduced in IFCMPS. The hardware results are consistent with the IFSMPS simulation results. The downside of IFSMPS is the more hardware components due to interleaving the converters.

The scope of the present work is the comparison of P.I.-F.O.P.I.D and FLC-FL controlled closed-loop IFSMPS systems. The comparison of the PFC using TNW and NLC-controller will be done in the future.

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