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A Simple Control Strategy Using Speedy Transient Response for Multiphase Buck Converter

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A Simple Control Strategy Using Speedy Transient Response for Multiphase Buck Converter

K Sasikala[1], D Ravikumar[2] and B Rubini[3]
[1, 3]Assistant Professor, Department of Electrical and Electronics Engineering, Vels University, Chennai, India.
[2] Assistant Professor, Department of Electronics and Communication Engineering, Vels University, Chennai, India

E-mail: sasikala1410@gmail.com

Abstract. The high performance of recent originating digital processors requires power supply for transient output, firm voltage regulation and high current. Industry has taken up interleaved multiphase synchronous buck converters for meeting such demands. Application of the voltage mode (ripple) hysteretic strategy to multiphase Voltage Regulator Units (VRU) would help satisfying many of the upcoming digital processors and IC's powering demands. This arises from the use of the various advantages that can be obtained from this technique. This current division method is known for several benefits it provides: easy accessibility in application to all control methods, with freedom from the prime control technique in voltage regulation loop, absence of any necessity for current reference, better accuracy in current division of equal magnitude at almost every load conditions in standstill and transients. As against this, there are several challenges that involve distribution of multiple control signals, current sharing and sensitivity to noise, high speed comparators, hysteretic band accuracy and stable at large load transients. In addition, application of the current division technique presented was made to a multiphase voltage mode ripple controlled Buck Converter that produced a novel and easy control strategy having minimum output voltage ripples and speedy transient output.

1. Introduction

There is a need for DC-DC converters and Voltage Regulator Units (VRU) for the future origination of IC's for digital processors that are inclusive of large current capability ,small output voltage variation in standstill and transient conditions, better power and current densities , light weight, miniature in size and greater efficiency[1],[2],[3]. There is an imperative need to get all these requirements satisfied at very low output which may drop below IV in the following years.

The interleaving (multiphase) and the single phase voltage mode (ripple) hysteretic control strategy have the ability to bring down the output voltage ripple to a greater value. But, there is still the need for investigation of the overshoot and undershoot demands during transients of higher magnitude [4]. Obtaining low output overshoot involves the requirements of the design of better operation feedback control from the multiphase VRM's. Such feedback control should have the ability to provide current sharing [5]. This is the reason why a vigilant control design in the output capacitor size is required for satisfying the maximum overshoot as well as undershoots limits during heavy load transients, despite the reduction of ripples in the output voltage and assistance in attaining speedy current transient output

coming from interleaving techniques[6]. It is possible for the hysteretic window to be placed to aelucidated level in the single phase ripple voltage mode control strategy. This is for ensuring speedy response from the controller to transitory load and correcting the voltage prior to variation in the undershoot and overshoot values. Despite the output capacitor still playing a significant role, there is a noticeable reduction in its size arising from hysteretic control.

There are many advantages seen in voltage mode hysteretic strategy over many other techniques. Those include easy accessibility, absence of necessity for closed loop compensation, an almost quick reaction to load changes and absence of any constraints on large frequency output voltage ripple having small switching frequency, identical current sharing (division) among the phases gives greater current carrying capacity and speedy transient output.Besides voltage regulation, high performance and current sharing functionality is needed from multiphase converters for ensuring almost identical division of load among the phases at almost every load conditions. The paper presents a multiphase voltage mode (ripple) hysteretic controlled Buck converter with current division technique.

2. Interleaved Buck Converter Using Voltage Mode (Ripple) Hysteretic Strategy

The below mentioning points require careful attention at the time of application of the hysteretic (ripple) voltage mode strategy to interleaved converters

(i) Frequent division has to be made for the control signal derived from the hysteretic (ripple) control, simultaneously maintaining the original control signal (interleaving).

(ii) Multiple control operation has to be disabled during transients to enable simultaneous switch ON andswitch OFF for the switches of all the phases. The converting frequency is a minimum to achieve the speedy transient output and identification among the phases at the time of transients.

Figure 1 is the functional diagram of N interleaved DC-DC converter using voltage mode (ripple) control strategy. Generating of the control signal (Cm) is to calculate the output voltage at a maximum value (VH) and minimum value (VL) to create a periodic window. The starting pulses between the phases is done to ensure that one phase upper sided switch is in the ON state at a particular time, but with all the remaining switches are being in the OFF state during the same time which generates the multipurpose control signals C1, C2, C3……CN.

As comparator 1 in a conduction state, the other comparator has the threshold limit of VLT<VL switches ON and all the upper side of a switches is (MOSFETs) and switches OFF of all the lower side of a switch is at a lower to higher load transients (thus the voltage undershoot).The new Threshold (VLT) is involved to ensure the transient output to produce speed at a maximum identify current sharing at ephemeral state. With no addition of this threshold, only one switch is in ON state at lower to higher ephemeral state when Vo<VL with the result of a slower transient output. On the other hand, every upper side switches are in the OFF state at a higher to lower load ephemeral state (those create potential overshoot) by the hysteretic comparator with new threshold which is larger than VH.

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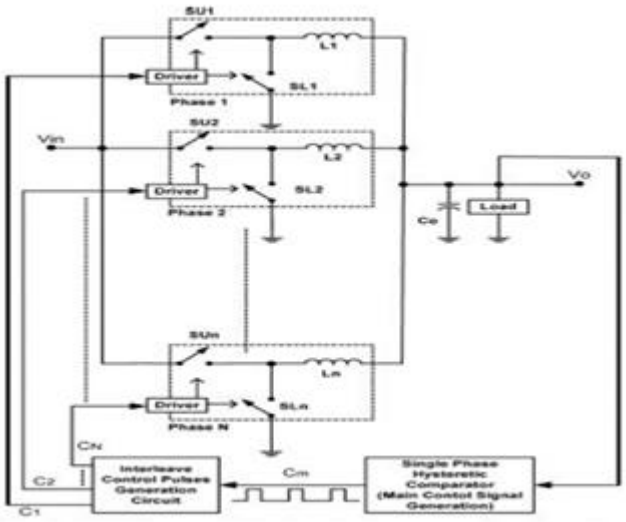

Figure 1 Functional Diagram of N interleaved converter using voltage mode (ripple) hysteretic control

3. Multiphase Voltage Mode (Ripple) Hysteretic strategy using Current Sharing (Division) Method

Identical distribution of the current between the phases at a multiphase converter is an important point to note. Unfortunately, there is a contingency of the components, connections and lay out deviations that cause inequality at a current distribution (sharing), more particularly at a large load transients.

Achievement of current division between the interleaved converters generally becomes a fast control over ON time at a converter phase. The ON time of particular phase carrying larger current is lesser compared to the ON time of other phases. It is also a way that the phase carrying the lowest current has the highest ON time. This implies that the current sharing (division) regulation is achieved by abridging the ON time of (phase) switches. There is the dependence of the current sharing (division) task on the control procedure that finds to use in the voltage regulation. Additionally, complexity is found for the current sharing functionality over and above the direct loop to the closed loop design. The ON time of the switches is a direct derivative from the ripples in the output voltage through fastening of the switches OFF/ON's with the output voltage hitting the upper as well as the lower constraints of the hysteretic comparator.

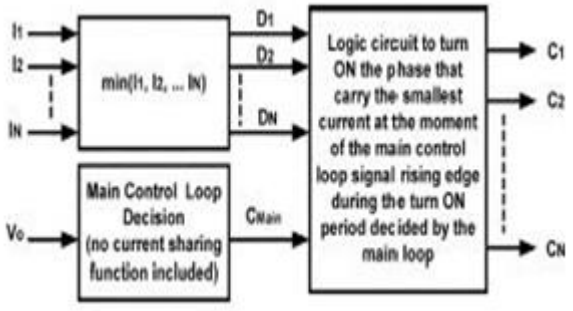

Figure 2 Basic functional diagram of the Proposed Method

Therefore any change in ON duration of a phase switch involves change in the hysteretic window of other switch that is turned ON indirectly. When the other switch is ON, numerous turn ON's are happened inside the comparator whose switching time period resulting in a higher switching frequency for each and every phase.

Figure 2 is the basic functional diagram of the proposed current sharing (division) method where the instantaneous currents at every phase are senses (I_1, I_2, I_3….I_N) and each compared to the another phases of instantaneous currents to produce the comparison digital code (D_1, D2, D3,….D_N), without any necessity for a allusion to identify the phase that carries the minimumcurrent. As the main regulating control loop having zero current division function determines the time to switch ON a switch, the upper sided switch in the converter for instance, furnish energy to the output of the converter. The phase that has the lowest current is switched ON through the introduction of a rising edge signal (C_{main}), while the remaining phases are switched OFF generating the terminal control signals (C_1, C2, C3……C_N).Stated in elementary languages, one switch is switched ON at any point of time. The choice of this switch is done through monitoring of the specific phase that is seen having the lowest instantaneous current during when a switch needs turned ON.

Despite the instantaneous comparison of current in every phase in relation to other phases on a continuous basis, decision on the comparison takes the effect at an increasing effect of the original control signal (C_{main}) by switching ON to the suitable phase. Therefore, the instantaneous position switch is the only effect on the current sharing process. Several methods are used for sensing instantaneous currents. One of the standard methods is through the inductors placing resistors in series having a small value. this is known for the simplicity and relative accuracy, downgrades is a result of the drop in the current sensing resistor, more particular applications involves more current. A second method is realizing the potential across the lower side switches.

i) Availability of the instantaneous current data for a DC-DC converter where the lower sided switch is in the ON state and the upper sided switch is in the OFF state.
ii) All the lower sided switches are ON period to turning ON one upper sided switch, resulting in the availability of the current information.

Figure 3 is the fundamental diagram meant for the multiphase voltage mode (ripple) hysteretic controller using the proposed current division technique. Figure.4 shows the conventional waveform samples meant for current division (sharing) process in a steady state. The basic working principle of the circuit is given in Figure.3 which can be elucidated with the related waveforms depicted in Figure.4. Generation of the main control signal (C_{main}) is done through comparison of the voltage at the output with a least voltage V_L and highest voltage V_H, approximating to a reference voltage V_{Ref} with the use of hysteretic comparator Comp2. The rising edge of the turn ON signal of $C_{main}$is utilized as a clock for D Flip flop causing activation of current sharing (division) decision of Comp1. A lower limit $V_{LT}<V_L$ is shown for Comp 3. The output of the comparator is logic 0 (low) in the standstill operation when$V_0>V_{LT}$ and logic 1 (high) during start up and also during the lower to higher load transients. $V_0<V_{LT}$ is the cause of the current sharing decision of Comp1.

Comp 3 has a lower limit $V_{LT}<V_L$. The output of the comparator is logic 0 at the time of standstill working when $V_0>V_{LT}$ and a logic 1 at the time of startup when $V_0<V_{LT}$ that is responsible for the phases to switch simultaneously at the time of transients. This process generates the required control signals C_1 and C_2 for achieving voltage regulation in addition to current sharing

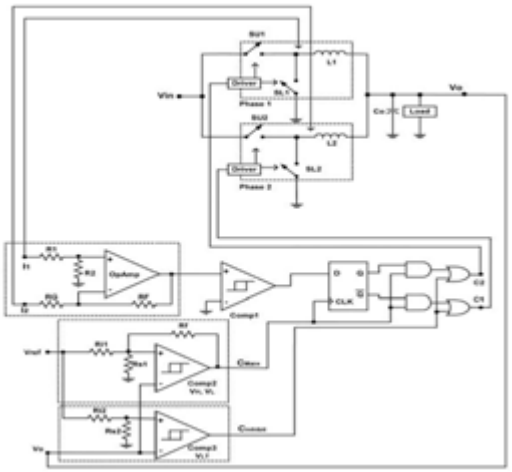

Figure 3 Proposed hysteretic Controller method

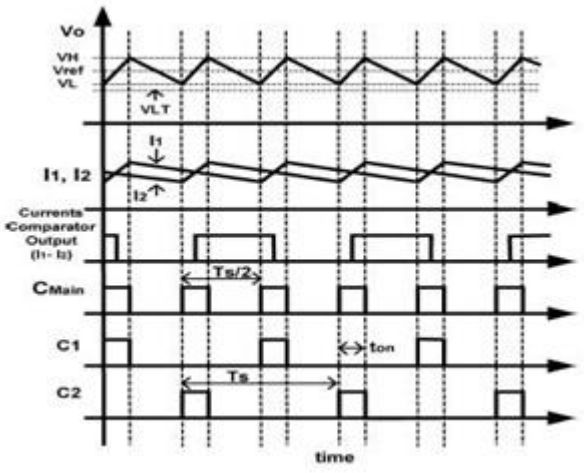

Figure 4 General waveform samples for the current division method

4. New control technique for n interleaved phases

Figure.5 is the basic widely used controller diagram for N multiphase voltage-mode (ripple) hysteretic strategic current division converters. Figure.5 depicts the outputs D_1,D_2……,D_N of the circuit using current comparison as a logic high at a time, making the phase carrying the lowest instantaneous current to switch ON at the rising edge of the voltage mode control loop as elucidated in the preceding part of the two-phase method[8].

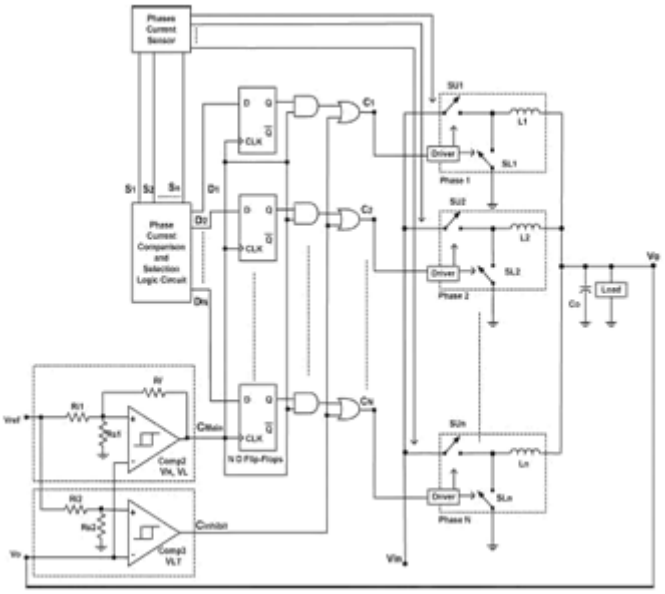

Figure 5 Fundamental controller diagram of N multiples of voltage-mode (ripple) hysteretic strategic current sharing (division) converters.

5. Theoretical analysis

This section carries an analysis of hysteretic controlled buck converter in a multiphase voltage-mode. The frequency equation is also obtained. There are certain assumptions made during the analysis. One is the buck converter is in standstill condition. Another is that all components are perfect with the exception of the following non idealities: The output capacitor consists of an identical Inductance (ESL) and identical Resistance (ESR), the switches have ON inductor and the resistance. There is an assessment that the voltage at the input is stable having zero ripples and the control loop having limited time duration [9].

Figure.6 depicts the voltage across the output capacitor in a stand still state considering ESL and ESR of the capacitor. In standstill state, the ripple voltage across the capacitor considering ESL and ESR is written by

$$v_{ripple}(t) = v_C(t) + v_{ESR}(t) + v_{ESL}(t) \quad (1)$$

Where

v_{ripple} (t) = Capacitor output voltage ripple

v_C(t) = capacitor output voltage;

v_{ESR} (t) = capacitor output voltage having Equivalent Resistance

v_{ESL} (t) = capacitor output voltage having Equivalent Inductance

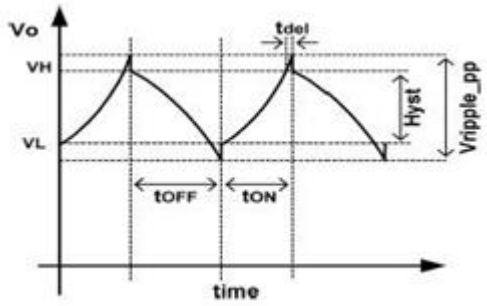

Figure 6 Output Voltage with its Ripple and delay time

In standstill condition two modes of operation are possible. At the time of Mode 1, as one of the upper -side switches in the ON condition, (1) turns

$$v_{ripple\_}ON\ (t) = \left(\frac{\Delta I \times t^2}{2 \times C_O \times D \times T_S} - \frac{\Delta I \times t}{2 \times C_O}\right) + \left(ESR \times \left(\frac{\Delta I \times t}{D \times T_S} - \frac{\Delta I}{2}\right)\right) + \left(ESL \times \frac{\Delta I}{D \times T_S}\right)$$

$$t_0 \le t \le DT_S. \quad (2)$$

At the time of Mode 2, as all upper-side switches are in the OFF condition, (1) is written by

$$v_{ripple\_}OFF(t) = \left(\frac{\Delta I \times t^2}{2 \times C_O \times (I-D) \times T_S} + \frac{\Delta I \times t}{2 \times C_O}\right) + \left(ESR \times \left(\frac{\Delta I}{2} - \frac{\Delta I \times t}{(1-D) \times T_S}\right)\right) + \left(-\frac{ESL \times \Delta I}{(1-D) \times T_S}\right)$$

$$DT_S \le t \le T_S \quad (3)$$

Where

ΔI = N phase overall inductor's current ripple;

T_S = N phase switches period;

D =duty cycle

C_O = N phase total output capacitance

The hysteresis window is then given by

$$H_{yst} = v_{ripple\_}ON\ (t_{ON\_}t_{del}) - v_{ripple\_}OFF\ (t_{OFF}\text{-}t_{del}) \quad (4)$$

Where

H_{yst} =hysteresis window;

t_{ON} =upper side switches ON time, where $t_{ON}=DT_S$;

t_{OFF} =upper side switches OFF time, where $t_{OFF}=(1\text{-}D)\ T_S$;

t_{del} = feedback loop's overall time delay.

Assume all the output inductors are symmetrical in all the phases, now the overall ripple current of inductor(s) having N phases is written by

$$\Delta I = V_{in} - I_0 R_{eq} - N V_O \times D \times T_S / L \quad (5)$$

Where

V_{in} = input voltage; V_O = output voltage;

R_{eq} =total path resistance;

L =output inductor of single phase

$$D = \frac{tON}{Ts} = \frac{V0 + I0/Req}{Vin} \quad (6)$$

The switching (changing) frequency relies on the current flowing through the load; this leaning is constrained, considering the same equivalent circuit of synchronous rectifiers over the switch period[7]. However there is a decrease in switching frequency with increase in the phases for the symmetrical hysteresis window. As a matter of fact, the output voltage has a smaller ripple when each phase's switching frequency maintains the same as that of N phase.

6. Simulation Results

Simulation of two-phase using the proposed current sharing method for DC-DC buck converter and hysteretic control was obtained. The design specifications include: Vin = 12V, V_0 = 1.5 V, 50A full load, L_{phasel} =L_{phase2} = 1 mH, and C_o = 20µF, transient hysteretic band of 300µV and hysteretic band of 100µV.. There is an assumption of three capacitors being e paralleled with ESR = 8mΩ, ESL = 4.8nH. Another simulation parameters were t_{del}=100 ns and R_{eq}=10mΩ.

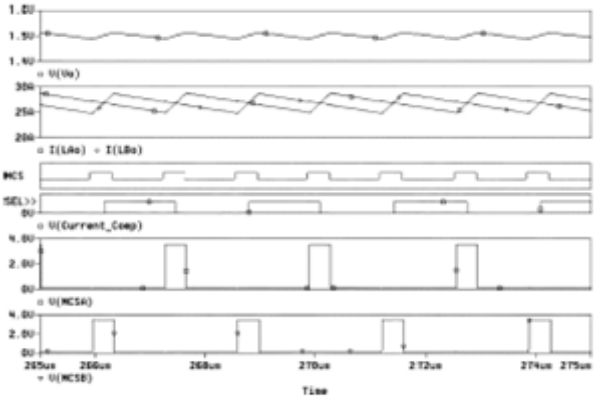

Figure 7 Simulation Results during the Steady-State condition

Figures 7-9 gives the outputs at different states. a) V (V_o) be the voltage output wave. b) I ($L1_o$) and I ($L2_o$) be the inductor output current wave for Phase 1 as well as Phase 2. c) MCS is the wave for output hysteretic comparator. d) V (Current Comp) be the current comparison waveform i) logic high when Phase 1< Phase 2 , ii) logic low when Phase 2<Phase 1. e) V (MCS 1) and V (MCS 2) is the upper -side switches driving waves of Phase 1 as well as Phase 2.

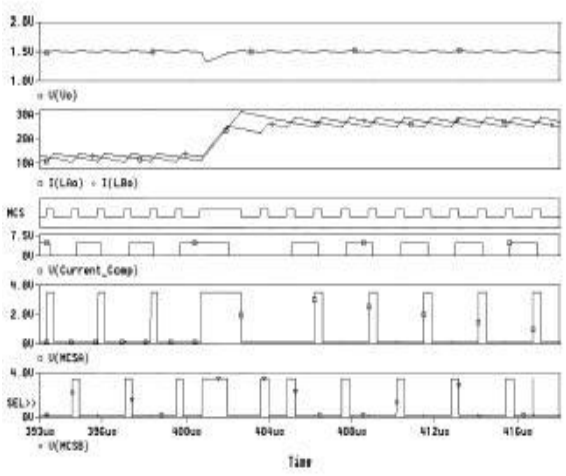

Figure 8 Simulation outputs in logic 1 to Logic 0 Load Transient State

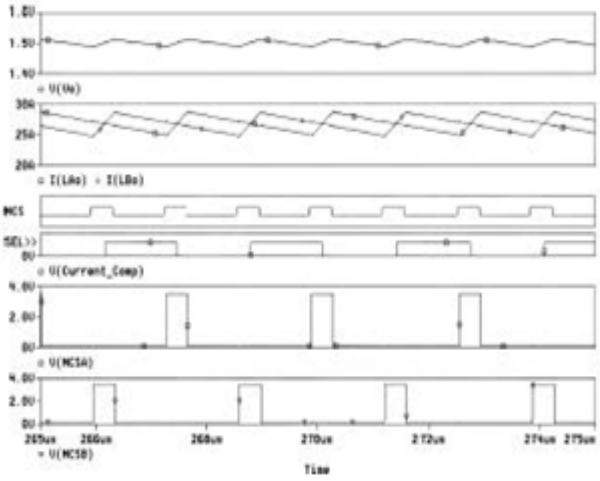

Figure 9 Simulation outputs in logic 0 to Logic 1 Load Transient State

7. Conclusion

This paper presents the current sharing method for multiphase voltage-mode (ripple) hysteretic strategy for DC-DC converters which has several advantages. These include simplicity in application, being free of the original control technique applied in the voltage regulation loop, absence of any necessity of current reference, better current sharing precision of equal magnitude at almost every standstill and transients load states, as a consequence not affecting the speed of the controller. In addition to the above conditions, there is another possibility of this sharing approach to any control method including events with no loop compensation like multiphase (ripple) hysteretic control. The implementation of the above method has been widely applied for N interleaved phases.

There is also some applications of this method to a multiphase voltage mode (ripple) hysteretic controller dc-dc converter, with the result of a recent and easy control strategy with low ripples in the output voltage and speedy transient output. The frequency equation has been found for N interleaved phases by including ESL, ESR as well as the path resistance with the output current effect.

8. References

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