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Area efficient LFSR based ADC in 45nm Technology using verilog a

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Abstract*— Data converters are very much useful in this modern world for circuit design at both ends i.e., transmitter end and receiver end. This paper primarily aims at reducing the overall area of the 8 bit ADC by decreasing the size of traditional counter with replacement of LFSR which uses few XOR gates and FFs. Another advantage of using LFSR is that it produce random states which may result in reducing the conversion time or in other words speeding up the ADC. Verilog A is used for implementing the ADC since it uses high level behavior model which allows to use simple equation to describe complex issues, a Standard language, Easy to learn and use and Flexible for both analog and AMS application Verilog A is much more simple than Spice C code. Linear feedback shift register is employed in the implementation of ADC as it fewer components than binary counter. The proposed ADC architecture is implemented and simulated using Cadence 0.45 µm tool and compared with Standard ADC which uses traditional binary counter. Results show that there is almost 50% in power savings when compared to the traditional ADC designs.

Keywords*— ADC, Area Efficient, Data converters, Verilog a, Linear Feedback Shift Register, Signal flow system.

I. INTRODUCTION

Analog signal to digital signal conversion is the method where a analog signal with continuous amplitude/time is transformed into a digital signal representation where amplitude and time are discrete. Translation is done from time to time with a period Ts or in terms of frequency Fs, and the amplitude is quantified into 2N levels, where N is the resolution of the Analog to Digital Converter. Currently there is a rising trend to build area efficient wireless sensors that are powered by battery or an energy harvester. Such devices can be used in quite a lot of applications, with different requirements for sampling rate, resolution, area and power consumption. Up-and-coming mixed signal applications such as radio-fz identification systems, WSN, transportable biometric equipments and energy hungry systems demand a area efficient, elevated power efficiency ADCs. A to D converters are one among the vital components used in the majority of such systems and usually use a fair share of the area.

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Amongst different analog to digital architectures, successive approximation register ADC [1-7] are the most accepted contender for the abovementioned applications which in general require high resolution, low area and low power.
Traditional Successive Approximation type ADC uses the standard binary search technique. The Advantage of using SAR ADCs is in medical field, such as pacemakers and cardiac defibrillators they strong requirements to power consumption and area to limit the no. of surgeries. Decreasing the power consumption of the device will not only add to the lifetime of the battery, but also give opportunities for alternative energy sources through energy harvesters. So to meet out low we go for using LFSRs

II. CURRENT STATE OF ART

Paper [1] The author has designed a low power 10 bit 5MS/s SAR ADC which reduces the area of capacitor array by 50% and reduction of switching power by 89% compared to the traditional one. Advantage of the capacitive DAC converter incorporated by this Analog to Digital Converter reduces parasitic capacitance as unique care is taken while forming the capacitor array.

Paper [2] The author has designed an area efficient CMOS 1MS/s 10bit charge redistribution SAR A to D Converter for measurement of battery voltage in a System on Chip. A new D to A Converter architecture which was used gave the benefits of low power with no application of the common mode voltage. The static power consumption was reduced by deployment of threshold inverter quantizer (TIQ) based Complementary Metal Oxide Semiconductor(CMOS) Inverter which was used as a comparator in the ADC. Sixteen level up shifters was deployed for converting the very low-core voltage control signals to the higher voltage level analog circuit in a 55nm CMOS process

Paper[3] Author proposed a new switching scheme for SAR ADCs. The recommended method attains 99.09% and 93.41% decrease in the average switching energy and area of capacitor when compared to the asymmetric capacitor array and splitted MSB capacitor. Likewise, the proposed SAR A to D acquires a reasonable linearity performance with maximum integral non linearity less than 0.112 LSB and maximum differential non linearity, less than 0.160 LSB and consume zero reset energy.

Paper [4] The author has experimented a 100 Gb/s communication with two Analog to Digital converters which is highly interleaved with interleaved sampling presented a voltage-based time model. Paper

Paper [5] The author has illustrated a 90nm cmos technology used for designing cascaded 5-bit two stage pipelined SAR Analog to Digital converter with 250 million samples per second which improves speed and improves power utilization.

Paper [6] The author has proposed a area efficient, low power 14 bit SAR (Succesive Approximation) ADC for array of sensors. A hybrid type capacitor DAC (digital to analog converter) comprises of a 10 bit split CDAC and a 5 bit serial CDAC utilized to decrease the area utilization. The overall requirement of unit capacitors is only 52.

Paper [7] The author has described a relative study of comparator and encoder in a 4bit Flash ADC for Pipeline ADC to attain a fast speed ADC. The traditional comparator was substituted with an open-loop comparator and non Read Only Memory type encoder is used as the substitute for the traditional encoder. It is implemented using 180nm Complementary metal oxide semiconductor technology.

III. VERILOG A

Verilog Analog Mixed Signal HDL allows designer of AMS design systems and ICs able to build and make use of modules and to use simple equation to describe complex issues. Mathematically behavior of all modules can be depicted in terms of its input ports and external output/parameters applied to the HDL modules. The structure of every element can be depicted in terms of interconnected sub-components. These descriptions can be used in many engineering disciplines such as electronic, mechanical, electrical, control, fluid dynamics, and thermo dynamics.

IV. NEED OF LFSR WHEN COMPARED TO COUNTER

For an N bit ADC (analog to digital converter) there will be 2^N possible digital outputs, which means that the SAR goes through maximum of 2^N states and so the number of Flip Flop required is N Flip Flops. For N bit SAR ADC structure requires N Flip-Flops and hence power consumption and area occupied is more since a few combinational Logic is required and hence power consumption is less and area occupied is also more. So LFSR is substituted in place of counters/registers since power as well as area is less compared to that of Conventional.

V. LINEAR FEEDBACK SHIFT REGISTER(LFSR)

The design of LFSR as counter is similar to that of the simple binary counter. LFSR has a Set signal whereas binary counter uses reset signal. Binary counters can be reset 0, but LFSR as counters are set to a value of all 1's but not to 0s. If LFSR acting as a counters set to all zero state, then they remain in the same state. In this work, LFSR as counters use XOR gates as feedback taps. The schematic of a 8 bit Linear Feedback Shift Register is shown in Fig. 4.

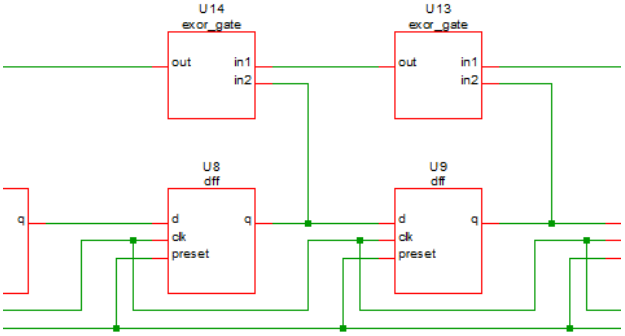

Fig.1. Linear Feedback Shift Register

VI. HELPFUL HINTS

The designed circuit architecture of analog to digital converter based on linear feedback shift register is shown in fig1. and the entire schematic is shown ing Fig.8 using Cadence tool. The analog input signal is first given to comparator along with reference voltage from output of DAC. The output of the comparator is given to control circuitry which drives the LFSR. The individual output of each flip flop is given to digital to analog converter (DAC). The digital to analog converter output is available at comparator where it compares with reference voltage and output is generated. The Cycle is repeated until the Comparator value is 0.

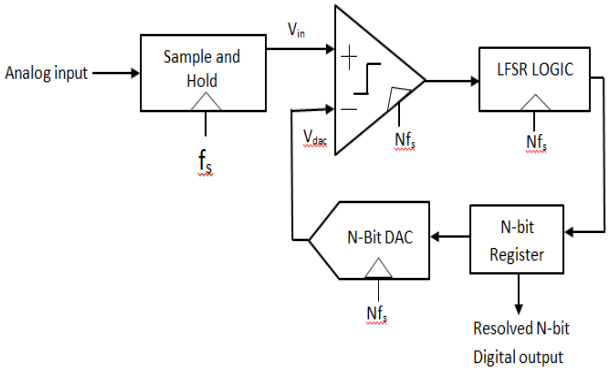

Fig.2. ADC Architecture

VII. LFSR BASED ADC

The proposed LFSR ADC based on pseudo random process. Fig.1 shows the proposed LFSR circuit. Fig.2. shows the proposed ADC architecture with LFSR. Working of the Proposed ADC is same as that of conventional ADC The usage linear feedback Shift Register aims to reduce area of ADC when compared to other circuits. The LFSR circuit has eight D-Flip-flop's where it generates 2^n-1 states that is 255 states (shown in fig.7) in the case of n=8. Here, The LFSR uses a polynomial function to produce maximum number of states, i.e.

$$PN(x) = x8 + x6 + x5 + x4 + 1$$

```
If (((v(ref)-v(in))>-0.5)&&((v(ref)-v(in)<9.4))
result=v(vss);
else
result=v(vdd);
v(out)<+transition(result,delay,ttime);
```

Fig.3.Snippet code of Comparator in Verilog-A

```
analog begin @(cross (v(clk),+1))
if(v(preset)>0)
result=1;
else
result=v(d);
v(q)<+transition (result,delay,ttime)
```

Fig.4.Snippet code of And Gate in Verilog-A

```
analog begin
if(v(q1)>0.5)
v1=128;
else
v1=0;
if(v(q2)>0.5)
v2=64;
else
v2=0;
if(v(q3)>0.5)
v3=32;
else
v3=0;
if(v(q4)>0.5)
v4=16;
else
v4=0;
if(v(q5)>0.5)
v5=8;
else
v5=0;
if(v(q6)>0.5)
v6=4;
```

Fig.5.Snippet code of DAC

The above proposed ADC architecture is implemented in Cadence Virtuoso Application Development Environment and Spectre Circuit Simulator is used in simulating the above proposed ADC architecture. All analog circuits are the comparator, and gate, LFSR, DAC as shown in the figure 2. The snippet code of each component is shown in figure 3,4,5,6. The potential bugs in Verilog-syntax are identified and rectified using Analog Hardware Description language Linter.

VIII. CONCLUSION

In this paper the proposed ADC architecture is designed and schematic is implemented in cadence using 45nm technology. Layout of the ADC is drawn and the area is calculated and compared with conventional ADC. Sampling was done at a rate of 25MS/S. Results shows that area was reduced by 50 percent when compared to conventional ADC implemented using same technology.

$$F(x) = \sum cnxn$$

TABLE 1. Comparison Between Proposed ADC Architecture and Standard ADC Architecture

	Proposed ADC	Standard ADC
AREA	0.272*0.47 mm^2	0.413*0.75 mm^2
POWER	~25µw	~48µw
Voltage	1.8 V	1.8 V
Sampling Rate, fs (MS/s)	25	25

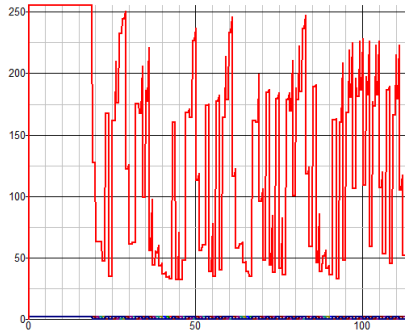

Fig.6. 255 Random States Produced By LFSR

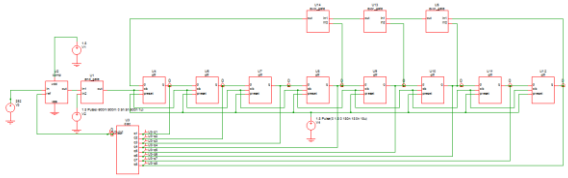

Fig.7. Schematic of ADC in Cadence

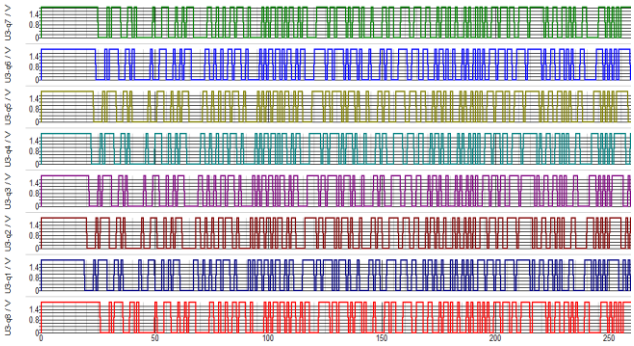

Fig.8. ADC Output stacked

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AUTHORS PROFILE

S.Karthik has completed his PhD in the area of VLSI.He has published more than 20 international journals.His research area includes High Performance computing, Reconfigurable architecture,VLSI Testing,DFT,Low power VLSI techniques. He has attended many conference and workshops throughout the world.He is well versed in HDLs like Verilog,VHDL.He has worked in many development board like PI,PYCOM,ZED.He was actively involved in projects such as low power pattern generation for BIST architecture, fault-tolerant architectures, dynamic partial reconfiguration in FPGAs, and low power adders. He believes in life-long learning. To update his skill set he has attended numerous training programs/workshops such as the Cadence training program, workshop in FPGA Based System Design using ALTERA EDA Tools and in Advanced Engineering Optimization and Modeling using MATLAB & SCILAB, just to name a few.

K.Priyadarsini has completed her M.Tech from VIT University. She was an Intern at CTS. She has worked in many IT companies has developer. She started her career at SRM University. She did her PhD from VISTAS. Her area of research includes High performance cloud computing, security aspects at Multicloud, data science. Data mining,Big data analytics. She has completed many online MOOC courses like Python for Data Science, Cloud computing . She is interested in Object Oriented Programming and carrying out workin building software models . She has published more than 10 international journals and she has presented many papers in conferences.

Sarat Suhas has completed his B.Tech from SRMIST,Vadpalani. His area of interest is embedded system, VLSI. His technical skills include Verilog, VHDL, System C. He has published two Scopus indexed journals. He has worked on many embedded boards like Raspberry PI, Arduino, Zybo, Pycom. He has participated in many technical events like quiz, paper presentation. He has done internships in core companies. He is working on dynamic clocking on embedded processors. He is well versed in Cadence tool like IUS,RTL Compiler,Nanorouter.He has done mixed signal projects using Verilog-A .His goal is to pursue MS in Electricla engineering with specialization in data science.