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Design and study of system on chip design for signal processing applications in terms of energy and area

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Abstract

Providing flexibility into a system on a chip design is sometimes required and generally always desirable. However the cost of providing this flexibility in terms of energy consumption and silicon area is not well understood. This cost can range over many orders of magnitude depending on the architecture and implementation strategy. To quantify this cost, efficiency metrics are introduced for energy (MOPS/mW) and area (MOPS/mm^2) and are used to compare a variety of designs and architectures for signal processing applications. It is found that the critical architectural parameters are the amount of flexibility, the granularity of the architecture in providing this flexibility and the amount of

parallelism. A range of architectural solutions which tradeoff these parameters are presented and applied to example applications.

Introduction

The tradeoff of various types of architectures to implement digital signal processing (DSP) algorithms has been a subject of investigation since the initial development of the theory [1]. Recently, however the application of these algorithms to systems that require low cost and the lowest possible energy consumption has placed a new emphasis on defining the most appropriate solutions. For example, advanced communication algorithms which exploit frequency and spatial diversities to combat wireless channel impairments and cancel multi-user interference for higher spectral efficiency (data rate/bandwidth) have extremely high computational complexity (10's–100's of billions of operations/second), and thus require the highest possible level of optimization.

In order to compare various architectures for these complex applications it is necessary to define design metrics which capture the most critical characteristics relating to energy and area efficiency as a function of the flexibility of the implementation. Flexibility in implementing various applications after the hardware has been fabricated is a desirable feature, and as will be shown it is the most critical criteria in determining the energy and area efficiency of the design. However, it is found that there is a range of multiple orders of magnitude differences in these efficiencies depending on the architecture used to provide various levels of flexibility. Therefore, it is important to understand the cost of flexibility and choose an architecture which provides the required amount at the highest possible efficiency.

Consequently, the flexibility consideration becomes a new dimension in the algorithm/architecture co-design space. Often the approach to flexibility has been to provide an unlimited amount through software programmability on a Von Neumann architecture. This approach was based on hardware technology assumptions which assumed hardware was expensive and the power consumption was not critical so that time multiplexing was employed to provide maximum sharing of the hardware resources. The situation now for highly integrated "system-on-a chip" implementations is fundamentally different: hardware is cheap with potentially 1000's of multipliers and ALU's on a chip and the energy consumption is a critical design constraint in many portable applications. Even in the case of applications that have an unlimited energy source, we are now beginning to move into an era of power constrained performance for the highest performance processors

since heat removal requires the processor to operate at lower clock rates than dictated by the logic delays.

The importance of architecture design is further underscored by the ever and faster increasing algorithm complexity, and purely relying on technology scaling many DSP architectures will fall short of computational capability for more advanced algorithms demanded by future systems. An efficient and flexible implementation of high-performance digital signal processing algorithms therefore relies on architecture optimization. Unfortunately, the lack of a systematic design approach and consistent metrics currently prevents the exploration of various realizations over a broad range of architectural options. The focus of this paper is to investigate the issues of flexibility and architecture design together with system and algorithm design and technology to get a better understanding of the key trade-offs and the costs of important architecture parameters and thus more insight in digital signal processing architecture optimization for high-performance and energy-sensitive portable applications.

Section 2 introduces the design metrics used for architecture evaluation and comparison with an analysis of the relationship between key architecture parameters and design metrics. Section 3 uses an example to compare two extreme architectures: software programmable and dedicated hardware implementation, which result in orders of magnitude difference in design metrics. The architectural factors that contribute to the difference are also identified and quantified. Section 4 focus on intermediate architectures and introduces an architecture approach to provide function-specific flexibility with high efficiency. This approach is demonstrated through a design example and the result is compared to other architectures.

Section snippets

Architecture space

The architectures being considered range from completely flexible software based processors including both general purpose as well as those optimized for digital signal

processing (DSP's), to inflexible designs using hardware dedicated to a single application. In addition architectures will be investigated which lie between these extremes.

Flexibility is achieved in a given architecture either through reconfiguration of interconnect between computational blocks (e.g. FPGA or reconfigurable

Software implementation vs. Hardware implementation for the same application

The previous section compared a variety of architectures under the condition of maximum possible throughput. This section will use a single application to give further insight into the reasons for the wide variation in efficiency.

Four multi-user detection schemes were evaluated in [3], which can be used in a wideband synchronous DS-CDMA system. The blind adaptive MMSE multi-user detector, which was one of those algorithms analyzed, will be used in this section since it gives the best trade-off

Architecture comparison and analysis

The comparisons of architectural implementations are shown in Table 4 and the breakdowns are depicted in Fig. 6. For the DSP implementations, since one processor cannot meet the throughput requirement, parallel processors are assumed and the overhead of splitting the algorithm into a number of processors is neglected for the upper efficiency bound of the software solutions. Notice the DSP extension can achieve considerable savings in both power consumption and area by increasing the data-path

Intermediate architectures

One of the main problems in the design of the hardware is a company dedicated to the prevention of the over-used, now is the lack of flexibility. This section provides an overview of our approach to this problem is to solve the problem. Flexibility is a desirable feature in many practical applications. For example, some of the functionality of a wireless system is a variable, and determine the application's requirements (e.g., data rate, and the minimum-error-rate), and the changes in the

Conclusion

Digital signal processing systems typically have hard real-time (throughput) constraints with flexibility as a required or desirable feature. The cost of this flexibility has been investigated and through the introduction of energy and area metrics the impact of unlimited flexibility has been quantified. It is seen that there is a range of up to 3 orders of magnitude in the energy and area inefficiency when full flexibility is compared to fully dedicated architectures. The architectural factors

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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